Design and Implementation of multilevel current source inverter topology with reduced number of switches

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Abstract: Current source inverters (CSIs) have some important features compared to Voltage source inverter. Simple control and inherent short circuit protection are main advantages of this current source inverter.Control of the CSI is similarly easier in grid -connected applications. As CSI can buffer the yield from voltage changes, produces a predetermined magnitude of current to the network and would thus be able to achieve high power factor. In addition, it has characteristic of short circuit protection. Current Source converters (CSCs) have been proposed and used in high-power applications. For example, adjustable speed drives and power grids, in view of some of benefits contrasted with its counterpart—voltage-source converters (VSCs). The power circuit of the CSI is simple due to absence of freewheeling diodes.The topologies need simple circuit to modify the modulation function of the level shifted PWM (LSPWM) scheme.The proposed configuration can work in two modes of operation depending on the values of current sources: symmetric and asymmetric. A comparision study of fifteen level CSI with thirty one level CSI is done in this paper. In comparison with conventional structures the proposed topologies have great improvement.

Keywords: Adjustable Speed Drives ,Current source converters(CSCs),Grid connected Applications,Level shifted PWM(LSPWM), Power Grids ,Voltage source converters(VSCs).

INTRODUCTION

High-performance semiconductor power electronic devices, such as metal-oxide semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), dual gate commutated thyristor (dual GCT) etc. have resulted in many researches on high-power converters, like multilevel inverters. Low value of total harmonic distortion (THD) and stress on inductors and switches, low dv/dt or reduced di/dt in high-power applications and reduced electromagnetic interference (EMI) noise are the substantial benefits of multilevel inverter. Several papers have been published on the MVSI to reduce the number of devices, to improve the number of voltage levels, to improve power rating and so on. However, a little attentiveness has to be given to MCSIs as they have major advantages when compared with the MVSIs in some of the applications. In addition, they are one of the best solutions to handle inverter output current harmonic and THD of the inverter. In high power applications, in which low voltage and high current are required, such as induction motor drives, static reactive power compensation, power systems, and grid integration of renewable sources, these current source inverters play vital role as MCSIs show reliable operation. Moreover, there is no need to have any overcurrent and the short-circuit protection in MCSIs. Voltage source inverter has shown intrinsic weakness for high power applications due to substantial switching losses and high dv/dt of the PWM operation leading to dangerous over voltages and electromagnetic interference problems. In high power areas, current source inverter using GTO has special interest. CSI is simpler as it has no freewheeling diode and has an uni-directional current flow. CSC can provide a higher reliability related with a dc link inductor than a capacitor for EVS an inherent overcurrent protection by current regulation of the controlled rectifier. In addition it is more efficient because of the quazi square wave and turn on and off only once per cycle of the output current. The multilevel CSI have been proposed to enhance the output current quality as well as to improve the output power level while keeping the switching frequency of the switch as low as possible. The capacitor filters also help to avoid the over voltage as in the motor. Multilevel CSI contribute to generate 30° leading angle for natural commutation of load commutated inverter. As the power rating of the induction motor is increased a large capacitance is required to create higher leading var requirement taken by the capacitor which could become unreasonably high the requirement of a large capacitor has limited the use of this drive for high power application. Control of CSI is comparatively simpler in grid connected application as CSI can buffer the output from the voltage fluctuations, produces a predetermined magnitude of current to the grid applications and can thus achieve a high power factor, its output current is less dictated by the grid voltage. Moreover it has inherent short circuit protection and advantage of rapid ness in system control.In order to suppress the source of harmonics that is the harmonic current on the DC side,the DC inductor is usually of large value so that the DC input current can be kept constant and the output current waveform is purely determined by the PWM signals. Many of the MCSI topologies have been evolved in the research, Paralleling three-level H-bridge current source inverter (CSI) cells, which is called CHB (cascaded H-bridge) . Cumbersome inductor and complexity of control system to balance the inductor's current are the basic problems related with these designs. The necessity of different isolated DC current sources is the disadvantage of this topology. These authors proposed another different MCSI utilising inductor cell associated with H-bridge. Unlike parallel MCSI, this design does not need many isolated DC current sources and complexity of control stratergy is moderated. However, costly, high volume, and multi rating inductor still exist.The main inverter that is the basic H-bridge produces a multilevel current waveform in cooperation with inductor cells present in parallel. An inductor cell has four unidirectional switches across an inductor in the cell circuit. The main aim of the inductor cells is to obtain the intermediate levels of output waveform without any external sources. However, adjusting the magnitude of inductor current is the main drawback of this circuit, especially when the number of inductor cells are more. Similarly, using inductor cells paralleled with H-bridge converter was presented and each inductor cell has four switches and two inductors. In order to obtain smooth DC currents, Bulky

inductors are used. Regulating the inductor currents and presence of discrete diodes connected in series with the power switches are some drawbacks associated with the CSI topology, which often degrade its efficiency. This circuit operates under low THD at low switching frequency due to the presence of the multilevel operation. In CSIs, disconnection may destroy the whole system; therefore, it is important to take a strategy to prevent from this issue. This paper proposes a new configuration based on two-switch modules and H-bridge converter. Regards to the value of the current sources in the modules, symmetric and asymmetric structures are achieved. One of the features used in the topology is the common emitter connection of the main switches which results in a simple gate drive circuit.

PROPOSED CURRENT SOURCE MULTILEVEL INVERTER

In this section a novel multilevel current source inverter is proposed. The important feature of MCSIs is the need of an unidirectional current switches which can be applied by a single diode less IGBT with a series connected diode. An AC capacitor connected in parallel with the load in this MCSI to play an important operation like a filter and also protects the converter from the current changes due to presence of the inductive component in the output current. The proposed topology has all the features of conventional structure. In addition, the proposed topology has some advantages like reduced number of switches, lower number of DC sources and also less implementation cost due to presence of common emitter connection of all the IGBTs when Compared with the conventional structure of multilevel current source inverter. On the basis of the value of the current sources, the proposed topology can be operated in two modes, one is symmetrical topology and the other is asymmetrical topology.

In symmetrical type the value of the current sources is equal and in the asymmetrical type, the value of the current sources should be different. The two cases are explained as follows.

OPERATION PRINCIPLE OF SYMMETRICAL MODE

The proposed symmetrical topology is shown in the figure with all the current sources having the same values. The proposed structure is formed by the current cells connection and the H- bridge inverter. Each cell has a dc current source and two power electronic devices i.e, IGBT, in which they on and off in a complimentary order. One of the switch is paralleled with dc current source. When the IGBT is turned on, the dc current source is present in the circuit and this particular cell does not involve in the output levels. Otherwise, the current cell injects the dc source to the output.

Let us assume that the maximum output current is I_{DC} , to produce symmetrical steps in the resultant output current, the magnitude of current sources should be considered as given below

$$\left\{ I_{DCi} = \frac{I_{DC}}{N_{source}} \;\middle|\; i = 1,2,\ldots\ldots\ldots N_{source} \right\}$$

Here number of sources are denoted by N_{source}. The current source is designed by using a Dc voltage source in series with the inductor. The value of current source is controlled by controlling the value of the dc voltage source. The series connection of Dc voltage source and the switch must be paralleled with a freewheeling diode for the purpose of uni-directional current.

In the proposed topology, positive levels are produced by the basic cells, and the negative levels are generated by using the H-bridge converter in which the switching frequency is low.

The number of output levels can be obtained from the formula given below:

$$N_{level} = N_{IGBT} - 3$$

The number of current sources required to produce N_{level} steps in the output current can be obtained from the formula given below:

$$N_{source} = \frac{N_{level}-1}{2} = \frac{N_{IGBT}-4}{2}$$

If the zero level is generated with the H-bridge, then the two unidirectional switches of the last module can be eliminated and the improved symmetrical structure is obtained.

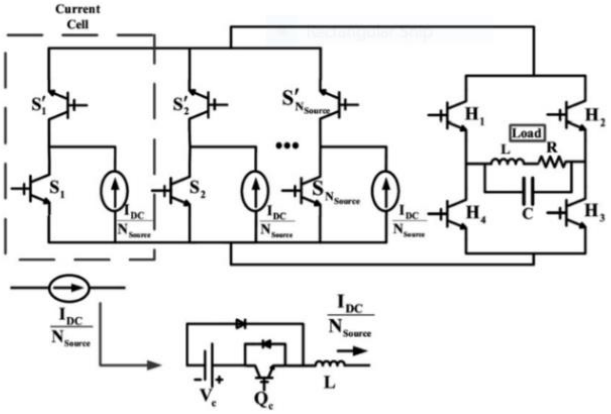


Fig.1 Proposed symmetric structure

Hence for the modified symmetric topology, the following equations are used to determine the number of levels and number of sources.

$$N_{level} = N_{IGBT} - 1$$

$$N_{source} = \frac{N_{level}-1}{2} = \frac{N_{IGBT}-2}{2}$$

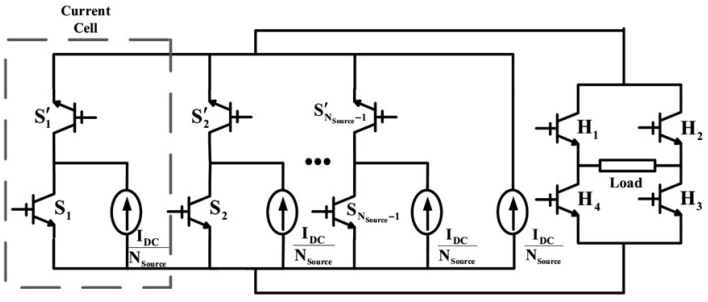


Fig.2 Modified proposed symmetrical structure

In th below figure, the PWM technique used in the topology is shown. Sinusoidal reference waveform and the level shifted carrier signals are compared and the desired positive levels are obtained and the negative levels are obtained by the H-bridge converter.

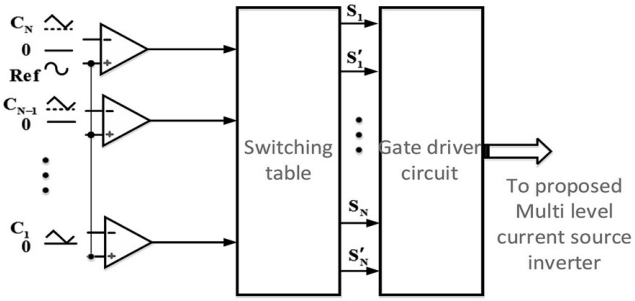


Fig.3 LS-PWM scheme for the proposed converter

Here N_{level} = 7 is considered to obtain seven level output currents $-I_{DC}$-level,- I_{DC}/3-level,$-2I_{DC}$/3 -level ,0 level, I_{DC}/3-level, $2I_{DC}$/3-level, I_{DC} -level. Here Dc sources taken are three and IGBT used are eight. Four of the switches are used to generate positive levels they are I_{DC}/3-level, $2I_{DC}$/3-level, and I_{DC} -level. The other four switches belonging to H-bridge illustrates the generation of various current levels.

The simulation results of the modified proposed topology of seven level symmetric CSI are shown below. The value of the current source is 0.35 A, Modulation index is 1, load used is 30+j3.14 ohm.

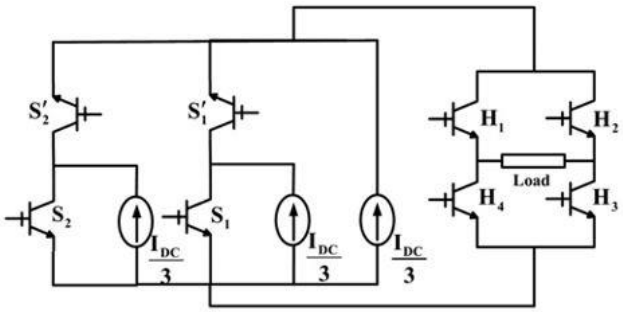


Fig.4 Modified proposed seven level MCSI

Table1:Switiching states of improved proposed seven level MCSI in symmetrical mode

Current level	switching states							
	S_1	S^1_1	S_2	S^1_2	H_1	H_2	H_3	H_4
$-I_{DC}$	0	1	0	1	0	1	0	1
$-2I_{DC}/3$	0	1	1	0	0	1	0	1
$-I_{DC}/3$	1	0	1	0	0	1	0	1
0	1	0	1	0	1	1	1	1
$I_{DC}/3$	1	0	1	0	1	0	1	0
$2I_{DC}/3$	0	1	1	0	1	0	1	0
I_{DC}	0	1	0	1	1	0	1	0

OPERATION PRINCIPLE OF ASYMMETRIC MODE

In the proposed Asymmetrical MCSI, the value of the current sources for each cell are different which can be seen from the figure. In order to achieve maximum levels in the output current, the value of the each current source used in the asymmetrical topology can be choosen according to the formula given below

$$I_{DCi} = \frac{2^{i-1}}{2^{N_{source}-1}}$$

Here I_{DCi} = the value of the ith cell's dc current source

I_{DC} = The maximum output current

The maximum value of the output current for the proposed asymmetric topology is given by

$$I_{OMax} = \frac{I_{DC}}{2^{N_{source}-1}} \sum_{i=1}^{N_{source}} 2^{i-1} = I_{DC}$$

$$N_{level} = 2^{\frac{N_{IGBT}-2}{2}} - 1$$

The above equation gives us the relation between the number of levels in the output waveform and the number of IGBTs. The relation between N_{source}, N_{IGBT}, number of levels is given by the following equations

$$N_{source} = (\log_2(N_{level}+1)) - 1$$

$$N_{IGBT} = 2\,[(\log_2(N_{level}+1)) + 1]$$

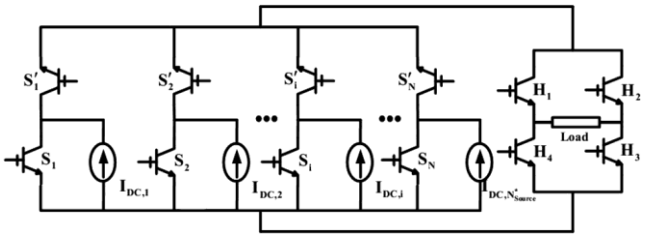


Fig5.Proposed Asymmetrical topology

Here for the fifteen level proposed asymmetrical topology, the number of DC sources required and the number of IGBT required are 3, 10 respectively. The PWM technique used is LS-PWM scheme. The value of the current sources are 0.35,0.7,1.4 A and the modulation index is 1 and the load used is 30+j3.14 ohm.

For Fifteen level : $N_{source} = (\log_2(15+1)) - 1) = 3$

And : $N_{IGBT} = 2\,[(\log_2(15+1)) + 1] = 10$

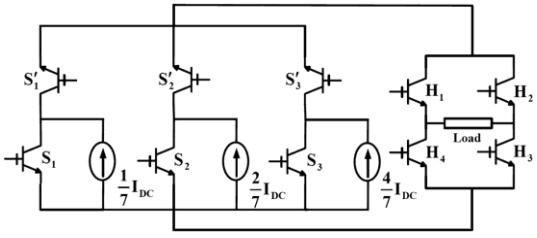


Fig6.Proposed fifteen level CSI

Table2:The switching states of fifteen level CSI are given below

Current level	Switching states					
	S_1	S^1_1	S_2	S^1_2	S_3	S^1_3
$-I_{DC}$	0	1	0	1	0	1
$-6I_{DC}/7$	1	0	0	1	0	1
$-5I_{DC}/7$	0	1	1	0	0	1
$-4I_{DC}/7$	1	0	1	0	0	1
$-3I_{DC}/7$	0	1	0	1	1	0
$-2I_{DC}/7$	1	0	0	1	1	0
$-I_{DC}/7$	0	1	1	0	1	0
0	1	0	1	0	1	0
$I_{DC}/7$	0	1	1	0	1	0
$2I_{DC}/7$	1	0	0	1	1	0
$3I_{DC}/7$	0	1	0	1	1	0
$4I_{DC}/7$	1	0	1	0	0	1
$5I_{DC}/7$	0	1	1	0	0	1
$6I_{DC}/7$	1	0	0	1	0	1
I_{DC}	0	1	0	1	0	1

PROPOSED THITRY ONE LEVEL MCSI:

The below figure shows the structure of thirty one level CSI. According to the formula,We used 12 switches and four current sources.

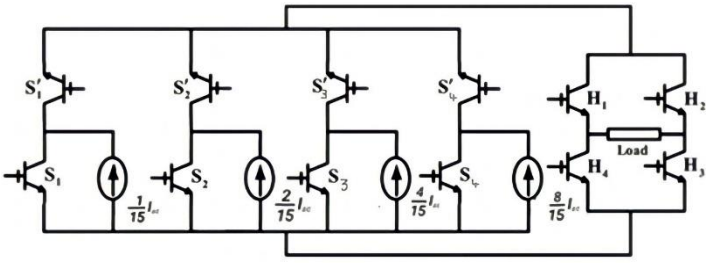


Fig7.Proposed Thirty one level structure

For thirty one level:

$N_{source} = (\log_2(31+1)) - 1) = 4$

$N_{IGBT} = 2\,[(\log_2(31+1)) + 1] = 12$

The magnitude of current source is 1/15 I_{DC},

$2/15I_{DC}$,$4/15I_{DC}$,$8/15I_{DC}$. For negative level H_2,H_4 and for positive level H_1,H_3 of the H bridge are on.

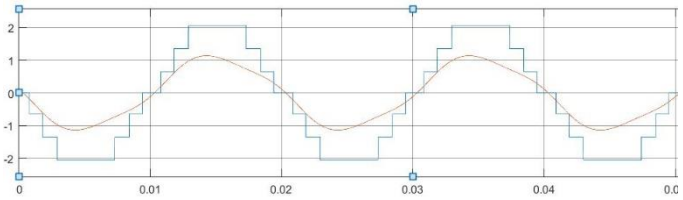
Here for the thirty one level proposed asymmetrical topology, the number of DC sources required and the number of IGBT required are 4, 12 respectively. The PWM technique used is LS-PWM scheme. The value of the current sources are 0.35,0.7,1.4,2.8A and the modulation index is 1 and the load used is 30+j3.14 ohm.

Table3:The switching table for the thirty one level CSI :

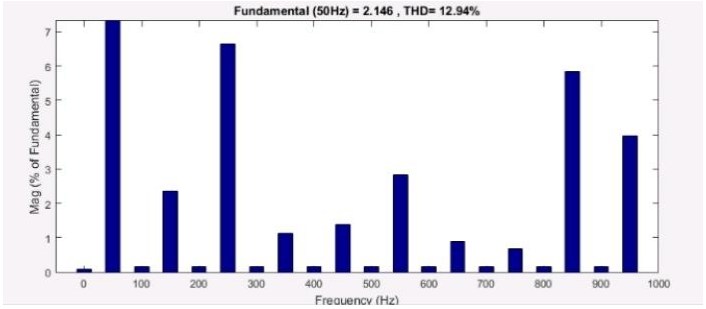
Current level	switching states							
	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'
$-I_{DC}$	0	1	0	1	0	1	0	1
$-14I_{DC}/15$	1	0	0	1	0	1	0	1
$-13I_{DC}/15$	0	1	1	0	0	1	0	1
$-12I_{DC}/15$	1	0	1	0	0	1	0	1
$-11I_{DC}/15$	0	1	0	1	1	0	0	1
$-10I_{DC}/15$	1	0	0	1	1	0	0	1
$-9I_{DC}/15$	0	1	1	0	1	0	0	1
$-8I_{DC}/15$	1	0	1	0	1	0	0	1
$-7I_{DC}/15$	0	1	0	1	0	1	1	0
$-6I_{DC}/15$	1	0	0	1	0	1	1	0
$-5I_{DC}/15$	0	1	1	0	0	1	1	0
$-4I_{DC}/15$	1	0	1	0	0	1	1	0
$-3I_{DC}/15$	0	1	0	1	1	0	1	0
$-2I_{DC}/15$	1	0	0	1	1	0	1	0
$-I_{DC}/15$	0	1	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0
$I_{DC}/15$	0	1	1	0	1	0	1	0
$2I_{DC}/15$	1	0	0	1	1	0	1	0
$3I_{DC}/15$	0	1	0	1	1	0	1	0
$4I_{DC}/15$	1	0	1	0	0	1	1	0
$5I_{DC}/15$	0	1	1	0	0	1	1	0
$6I_{DC}/15$	1	0	0	1	0	1	1	0
$7I_{DC}/15$	0	1	0	1	0	1	1	0
$8I_{DC}/15$	1	0	1	0	1	0	0	1
$9I_{DC}/15$	0	1	1	0	1	0	0	1
$10I_{DC}/15$	1	0	0	1	1	0	0	1
$11I_{DC}/15$	0	1	0	1	1	0	0	1
$12I_{DC}/15$	1	0	1	0	0	1	0	1
$13I_{DC}/15$	0	1	1	0	0	1	0	1
$14I_{DC}/15$	1	0	0	1	0	1	0	1
I_{DC}	0	1	0	1	0	1	0	1

RESULTS:

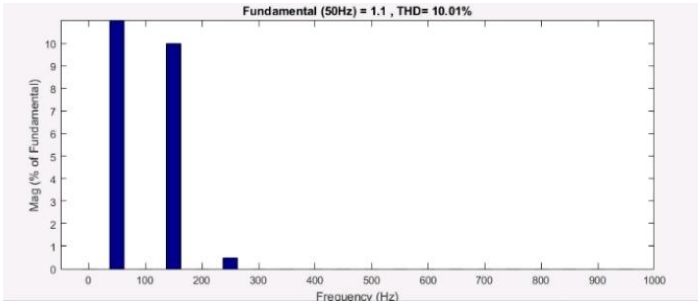
Simulation results of seven level MCSI



Waveform of Output Current and load voltage

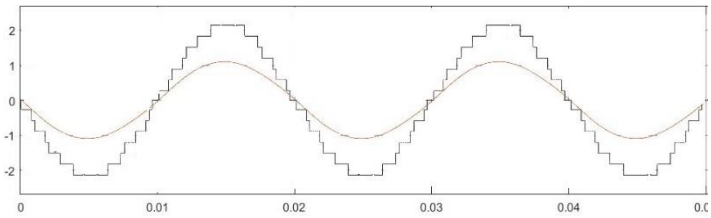


Harmonic spectrum of Output Current

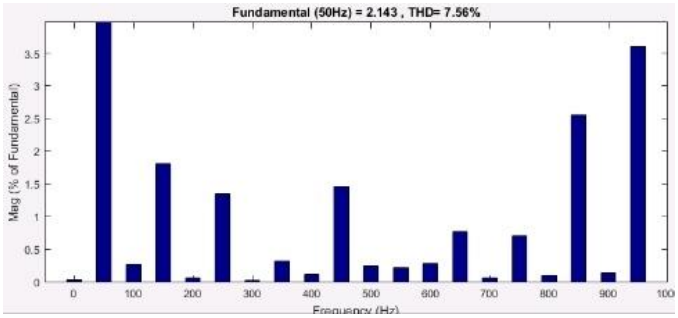


Harmonic spectrum of load voltage

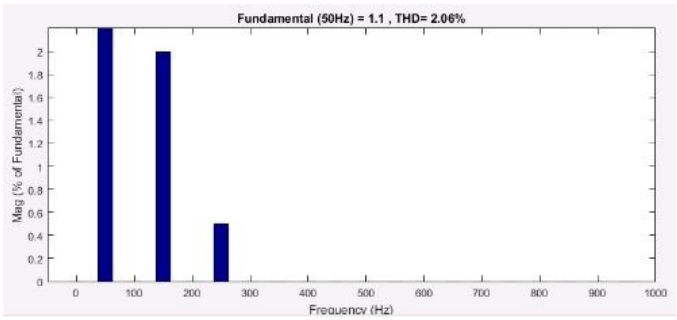
Simulation results of fifteen level MCSI



Waveform of output current and load voltage

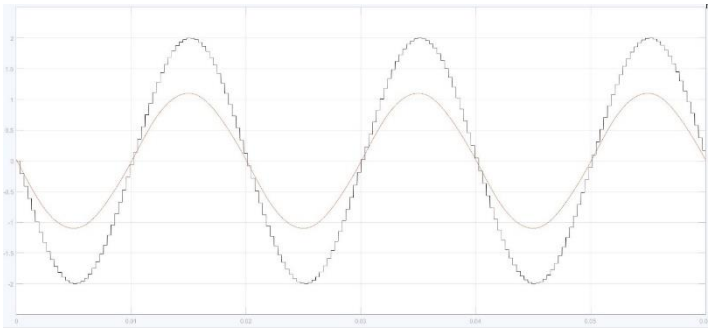


Harmonic spectrum of Output Current

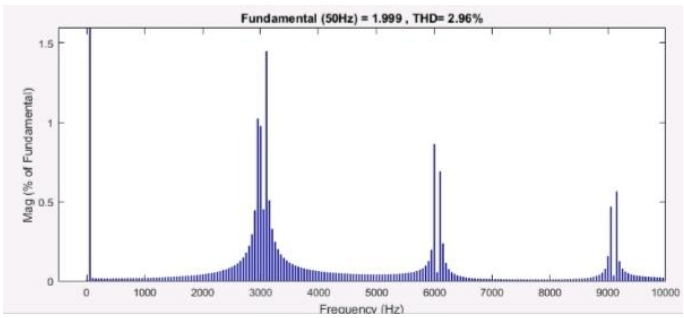


Harmonic spectrum of load voltage

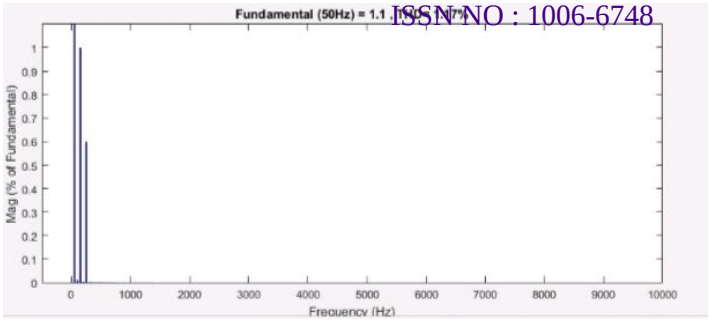
Simulation results of thirty one level MCSI



Wave form of output current and load voltage



Harmonic spectrum of output current



Harmonic spectrum of load voltage

DESIGN OF OUTPUT FILTER CAPACITOR:

The output filter capacitor plays two major roles in the current source inverters they are:

1.The filter capacitor is used for the flow of harmonic components present in the pulse width modulation currents.

2. As the load used in this is an inductive load, the sudden current changes are avoided by the filter capacitor.

In addition, as the inverter behaves as the constant current source, the equivqlent impedence that must be connected at the output stage of the CSI must be a capacitive load.

COMPARISION STUDY:

MCSI TOPOLOGY	SEVEN LEVEL CSI	FIFTEEN LEVEL CSI	THIRTY ONE LEVEL CSI
Number of IGBT's	8	10	12
Number of current Sources	3	3	4
Number of inductors	3	3	4
Total Harmonic Distortion in output Current	12.94%	7.56%	2.96%
Total Harmonic Distortion in load voltage	10.01%	2.06%	1.17%

CONCLUSION:

In this paper, symmetric and asymmetric multi level CSI topologies are proposed. A Seven level symmetric topology and fifteen, thirty one level asymmetric topologies are designed. This proposed CSI has a reduced number of switches and also reduced number of current sources in comparision with the conventional structures. This results in the reduction of cost of the coverter. And also the implementation and control is simple. Mainly in this paper, a comparision study of total harmonic distortion is done. By

increasing the number of levels, the total harmonic distortion is reduced and a nearly equal sinusoidal output waveform in thirty one level CSI is obtained that can be observed from this paper.

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