Comparison of level shifted pulse width modulation techniques for a single phase grid connected hybrid nine level inverter with the less number of switches.

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Abstract

The design and comparison of level shift pulse width modulated (LS PWM) techniques such as phase disposition, phase opposition disposition, and alternate phase opposition disposition are proposed in this paper. These techniques are implemented on a single-phase hybrid nine-level inverter topology. Implementation is done by generating ten input gate signals and introduced them into the new topology so that, nine levels of voltage are generated in the output. The new topology has better advantages than a conventional nine-level inverter, such as less number of switches, better output voltage waveform in sinusoidal form, less distortion, uniform loss distribution across all Insulated Gate Bipolar Transistor (IGBT) switches, reduced filter size, cheaper, high efficiency, and good reliability. The proposed three LSPWM designs are implemented on a hybrid nine-level inverter through MATLAB simulation and the output results are compared in this paper.

Keywords:- Level shift pulse width modulation(LSPWM), Phase Disposition(PD), Phase Opposition Disposition(POD), Alternate Phase Opposition Disposition(APOD), Alternate Current(AC), Multi-Level Inverter(MLI), Hybrid Nine Level Inverter(H9LI), Direct Current(DC), Insulated Gate Bipolar Transistor (IGBT)

I. INTRODUCTION

In the circuit with different switching actions, direct current is transferred into a particular branch in a bi-directional way, such that the branch experiences the alternate current flow in it. This phenomenon is known as inverter action. One can generate AC at any required voltage and frequency implementing various control strategies to the main circuit. The output waveform generated by an inverter is of two levels, if it generates more than two levels then it is treated as a multilevel inverter. An increase in the output levels leads to an increase in the switch count and more complexity.

To reduce complexity in the design and to be economical, the new topology introduces a short design for a Hybrid Nine Level Inverter (H9LI) with 10 switches for 9 level output. Whereas a conventional nine-level inverter uses 16 switches and contains complexity in the bulk design. Therefore, 16 switches are reduced to 10 switches in this paper. This paper also introduces the implementation of level shift control strategies on H9LI in simulation. Then observed the output waveforms in simulation with three control strategies, PD, POD, and APOD for H9LI using MATLAB software.

The main significance of this paper is to reduce the switch count and compare the designs of the three control strategies mentioned above.

II. Proposed System

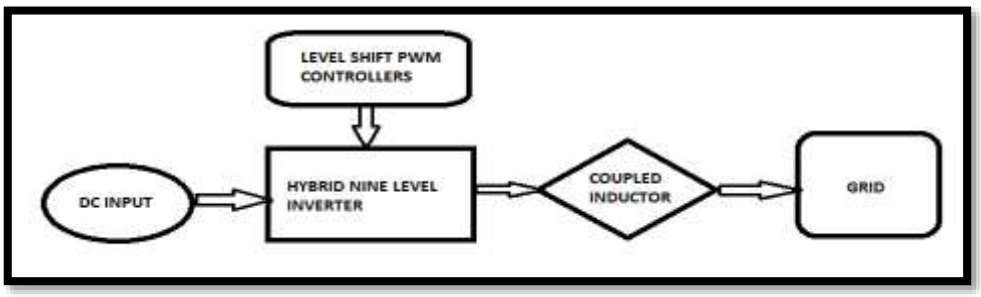

Fig 1 Block Diagram of the proposed system

Components of the proposed system

- DC input voltage(200V)
- Ten IGBT switches
- One auxiliary DC capacitor 'C_A' and two input DC capacitors 'C1, C2'.
- A coupled inductor (L1, L2)
- LS PWM control circuits
- 80V Grid-connected

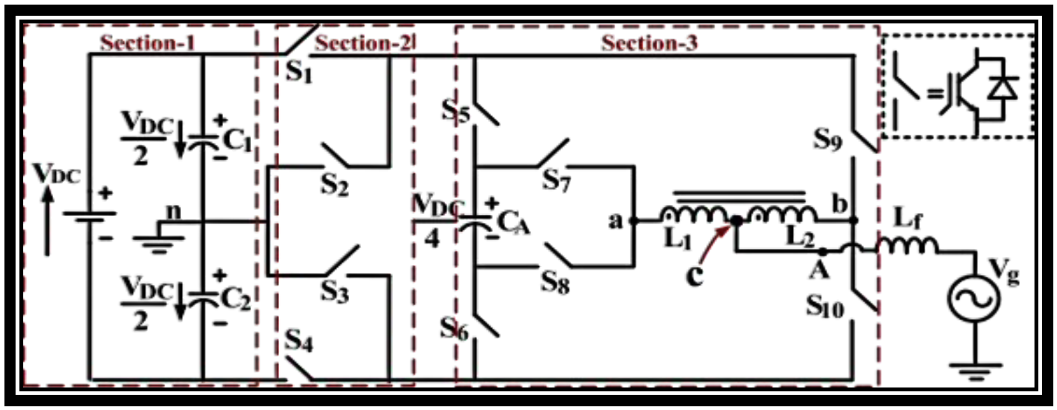

Fig 2 Design of H9LI power circuit

Coupled Inductor - The two coils which are coupled through electromagnetic connection is known as a coupled inductor. It has two input terminals and one output terminal**. It helps in the collection of the output nine-level waveform in a desired sinusoidal form.** It also decreases the filter size compared to the filter size of the conventional inverter by eliminating the usage of more dc capacitors.

To generate nine-level output voltage the circuit undergoes the sixteen different modes of operation by various switching actions as shown below the table.

SS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	V (out)
1	1	0	1	0	1	0	1	0	1	0	+4Vdc/8
2	1	0	1	0	1	0	0	1	1	0	+3Vdc/8
3	1	0	1	0	0	1	1	0	1	0	+3Vdc/8
4	1	0	1	0	0	1	0	1	1	0	+2Vdc/8
5	1	0	1	0	1	0	1	0	0	1	+2Vdc/8
6	1	0	1	0	1	0	0	1	0	1	+1Vdc/8
7	1	0	1	0	0	1	1	0	0	1	+1Vdc/8
8	1	0	1	0	0	1	0	1	0	1	0
9	0	1	0	1	1	0	1	0	1	0	0
10	0	1	0	1	1	0	0	1	1	0	-1Vdc/8
11	0	1	0	1	0	1	1	0	1	0	-1Vdc/8
12	0	1	0	1	0	1	0	1	1	0	-2Vdc/8
13	0	1	0	1	1	0	1	0	0	1	-2Vdc/8
14	0	1	0	1	1	0	0	1	0	1	-3Vdc/8
15	0	1	0	1	0	1	1	0	0	1	-3Vdc/8
16	0	1	0	1	0	1	0	1	0	1	-4Vdc/8

Table 2 sixteen switching states

SS – Switching States

Switching Conditions: 1 – ON, 0 – OFF.

To implement various switching actions, level-shifted pulse width modulated techniques are discussed in this project for H9LI. The three different types of LSPWM techniques are,

- Phase disposition PWM
- Phase opposition disposition PWM
- Alternate phase opposition disposition PWM

The H9LI obtains an n=9 levels in number in the output voltage waveform. Here in these techniques (n-1) carrier signals are used i.e., eight carrier signals. And also a reference signal is used. Then the comparison of carrier signals with a reference signal using comparators in the Simulink library leads to the required input signals generation.

III. Experiment and Result

Experimental parameters used in this proposed system are as follows,

1	INPUT DC VOLTAGE	200V
2	SYSTEM RATING	400VA
3	OUTPUT INDUCTOR	2mH
4	INPUT DC CAPACITORS	3300μF(C1,C2)
5	AUXILIARY CAPACITOR	3300μF(CA)
6	MUTUAL INDUCTANCE	4mH

Table 1 parameters used

- **Phase disposition PWM (PD PWM)**

  All eight carrier signals are in in-phase**.**

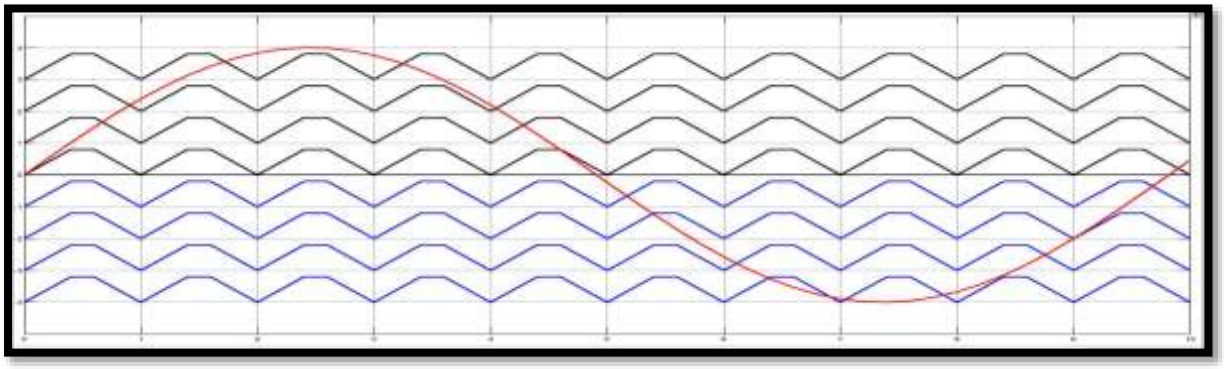

Fig 3 PD PWM graphical representation

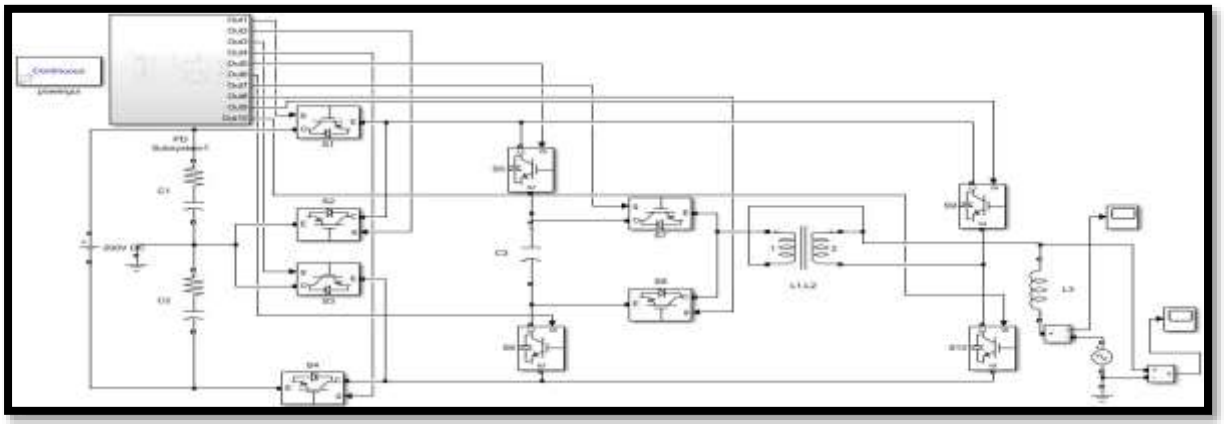

Fig 4 Simulink model of H9LI with PD

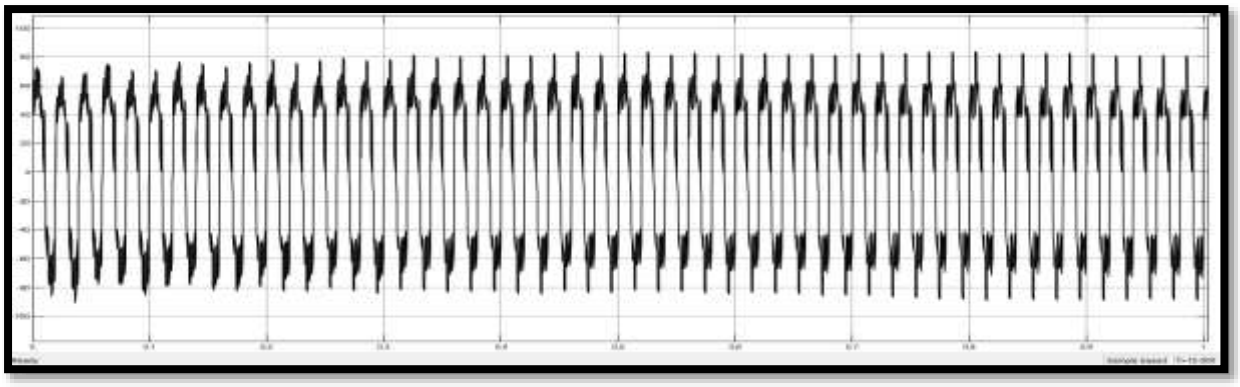

Fig 5 Output voltage with PD

- **Phase opposition disposition PWM (POD PWM)**

  (4,5,6,7) carrier signals are out of phase with the (1,2,3,4) carrier signals.

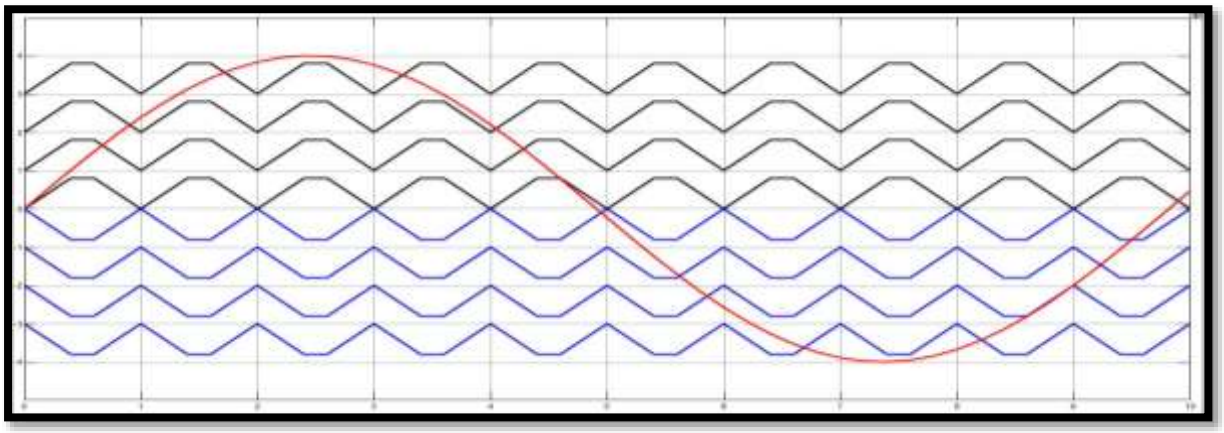

Fig 6 POD PWM graphical representation

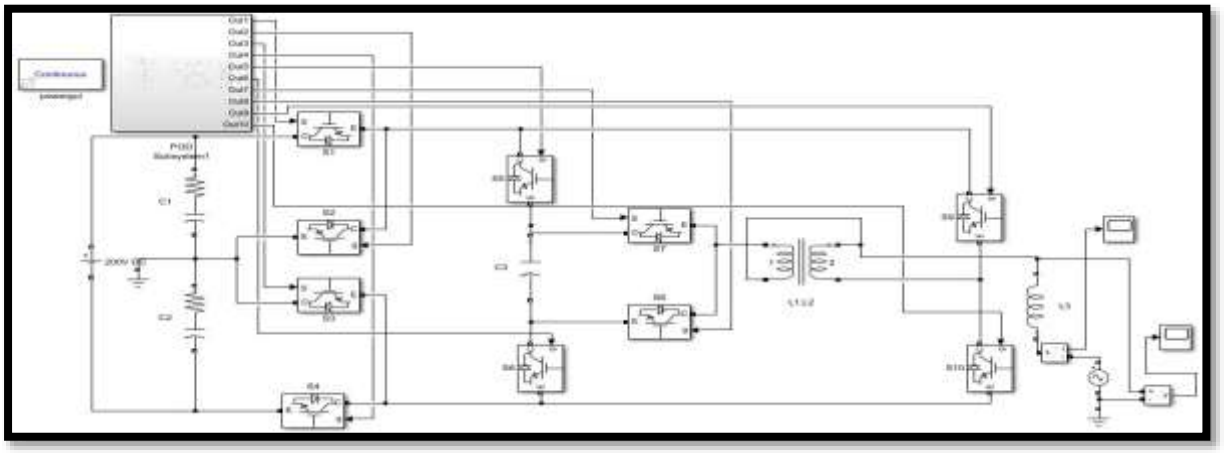

Fig 7 Simulink model of H9LI with POD

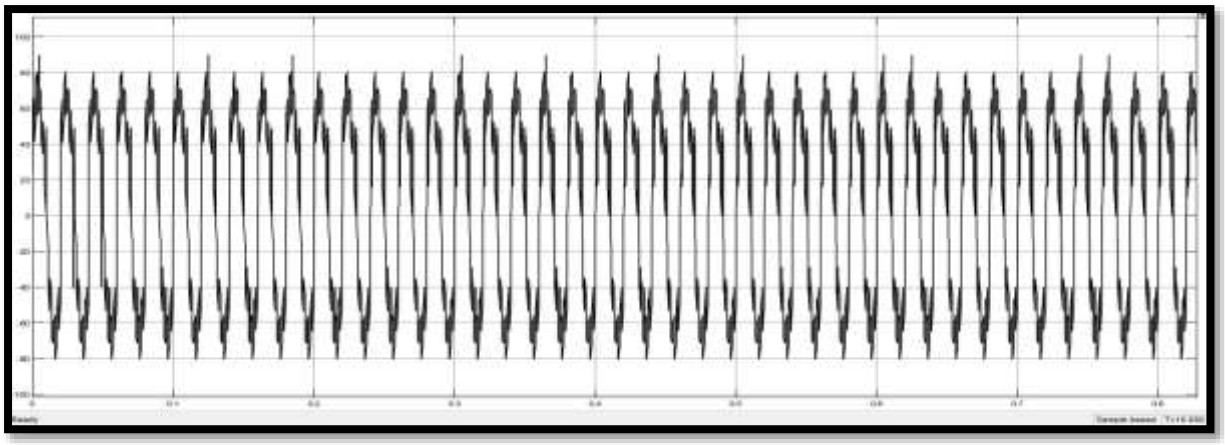

Fig 8 Output voltage with POD

- **Alternate phase opposition disposition PWM (APOD PWM)**

(1,3,5,7) carrier signals are in in-phase and other signals in out of phase.

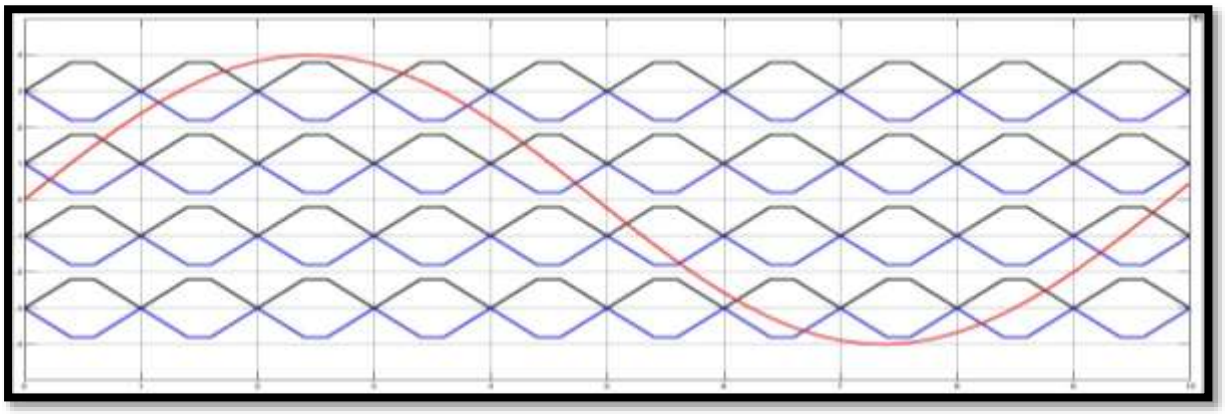

Fig 9 APOD PWM graphical representation

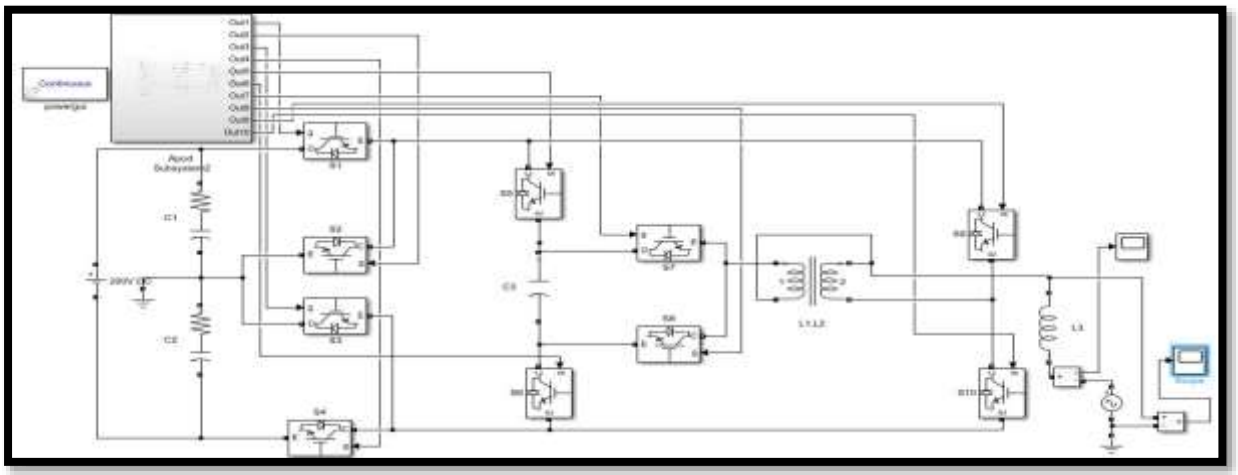

Fig 10 Simulink model of H9LI with APOD

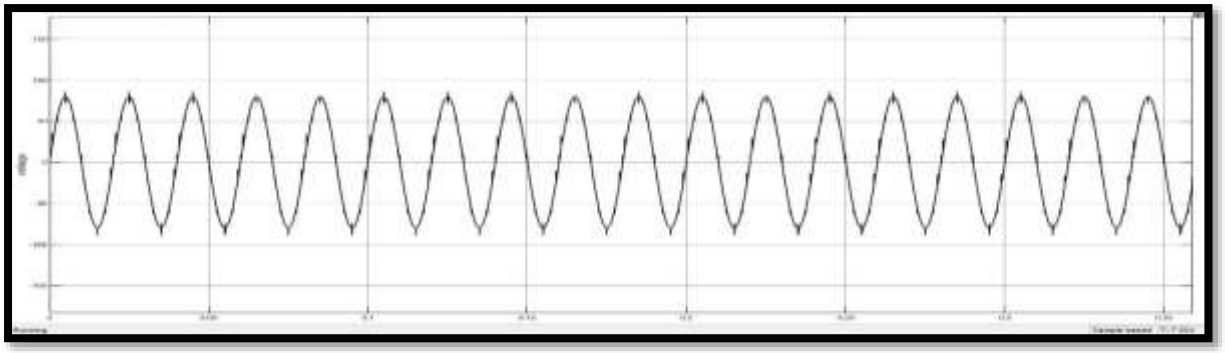

Fig 11 Output voltage with APOD

IV. CONCLUSION

The three control techniques of level shifted PWM like PD, POD, and APOD are designed and implemented with the new topology of hybrid nine-level inverter in MATLAB/SIMULINK simulation. From the obtained waveforms we can summarize the techniques such that the APOD technique is having better sinusoidal output waveforms compared to PD and POD techniques by observing the output waveforms in figures 5, 8, and 11. And circuit design is a bit complex for APOD comparatively because of alternate carrier signal analysis in comparators internally and usage of appropriate logic gates is typical. Output voltage levels increased (i.e., almost sinusoidal) due to the presence of a coupled inductor. The decreased number of components in the new H9LI topology leads to lighter and economic compared to a conventional nine-level inverter.

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