Two Inductor Non-Isolated Chopper Fed to Diode Clamped Multi-Level Inverter

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Abstract

An alternative non-isolated circuit breaker with a high voltage boost function fed to different levels of diode clamped multi-level inverter is proposed and THD'S at different levels are compared. The proposed topology of two inductors non-Isolated chopper Demonstrates the deserves of a better and wider variety of step-up voltage advantage whilst in comparison with the latest topologies. A diode clamped multi-stage inverter that offers excessive performance due to the essential frequency used for all the switching gadgets and this easy technique of again-to-again energy switch systems is fed with a non- isolated DC-DC converter. The efficient and compact design of multilevel inverters motivates various applications such as solar PV and electric vehicles. The total harmonic distortion was measured concerning various values of sinusoidal input in the PWM modulation scheme for each inverter.

Keywords- Two inductors non-Isolated dc-dc converter, Diode clamped multi-level inverter (DCMLI), Sinusoidal pulse width modulation (SPWM).

I. INTRODUCTION

The utilization of renewable electricity reasserts is growing each day to resolve the ever-growing electricity disaster for a sustainable future. The low output voltages and intermittency traits of renewable electricity reasserts may be alleviated with the aid of using the use of diverse step-up DC-DC converters. DC-DC converter presented in [1] for renewable energy conversion applications. The presented converter operated in closed-loop control. in [2] various kinds of inverter circuits were demonstrated explained. In [3]-[5] advanced z-source inviters were implemented for renewable energy conversion applications and reducing ripples in the DC supply side.

Boost converters are extensively being used in Solar PV systems as the solar PV generates a small amount of voltage, with numbers of cells connected in series, it will be able to generate 200-230V under the best possible operating conditions. In conditions like summer, its open-circuit voltage will drop in PV but when comes to the proposed two inductor chopper it gives a voltage gain of 20%. Thus boost converters are extensively utilized to meet the load requirements irrespective of the prevailing conditions.[3-4]

With the call for growth within side the necessities of high- electricity first-class in commercial packages and sun PV systems, the traditional inverters in assembly the preferred situations like a natural sine-wave output and much less harmonic distortions is a tough task.

The green and compact layout of multilevel inverters (MLI) motivates numerous packages consisting of sun PV and electric-powered vehicles (EV) in [5-7].The multilevel inverter configuration stands excessively [8-10] used in most high-power applications. The preferred alternating voltage level can appear at the output with numerous DC voltages at the input. In [6] and [13] inverters are used for power quality improvement. The presented topology is executed in simulation software. Diode clamped multi-level inverter are fed by Non-isolated chopper with an excessive voltage boosting functionality is proposed. So in this paper, when dc input is given to a non-isolated booster converter with a duty cycle of 70%, it gives a high voltage gain of about 23%. The obtained voltage at the chopper is given to different levels of DCMLI and THD's at those levels are compared.

II.Non isolated converter

A non-isolated converter, dc input, and output are connected to the same potential. These types of choppers are typically known as Buck, Boost, or Buck-Boost converters in [11-14].

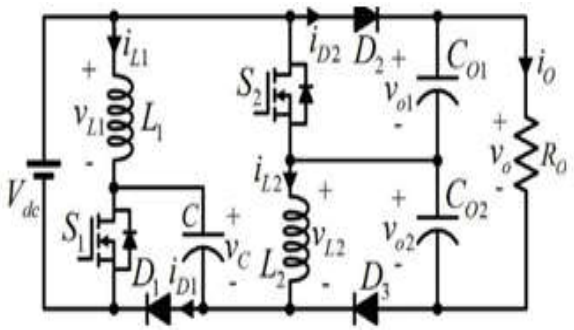


Fig. 1. Circuit diagram for non-isolated chopper

Fig.1 shows a non-isolated dc-dc converter. in this circuit, Two switches S1 and S2, a capacitor C, two inductors L1 and L2, three diodes D1, D2, and D3, and two output capacitors CO1 and CO2 make up the proposed chopper topology. Two inductors are used, one of which has its flux linkage increase during its charging period to achieve a high step-up voltage gain. One of the three integrated capacitors exhibits a partial switched-capacitor characteristic, while the other two are linked in series across the load. To generate a large step-up voltage gain, its two inductors are charged in parallel during the switched-on period and discharged in series during the switched-off period.The two series-connected output capacitors improve step-up gain, whereas C absorbs energy from L1 before it is passed to CO2 and L2. The switching capacitor technique encouraged the integration of C. The use of two output capacitors effectively minimizes the voltage stress on each capacitor when compared to topologies with only one output capacitor.The two power switch by the very same switching frequency, while L2 is charged towards the sum voltage across C and Vdc to boost 1 higher.

In mode 1:

The switches S1 and S2 are switched ON; Diodes D1 & D2 are in reverse biased and diode D3 is in forward biased condition.

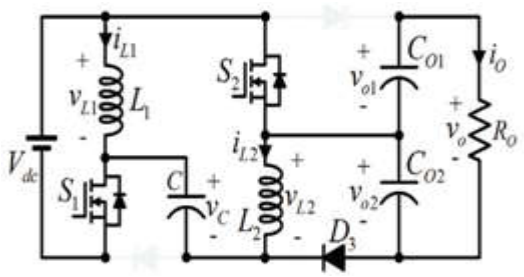


Fig.2. Mode 1 operation of Non-Isolated Converter Current flow: (i) +Vdc -> L1 -> S1 -> -Vdc

ii) +Vdc -> S2 -> CO2 -> D3 -> C -> S1 -> -Vdc

L1 and L2 both store the energy, while CO1 gets discharged through the load by supplying to it.

In mode 2:

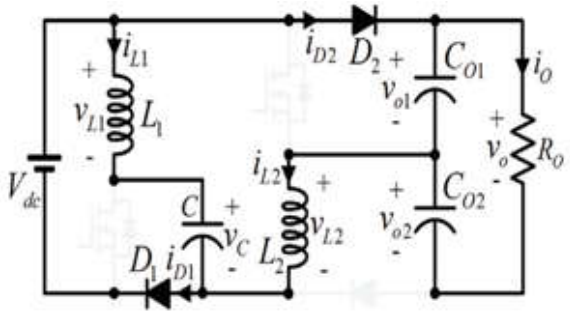


Fig. 3. Mode 2 operation of Non-Isolated Converter

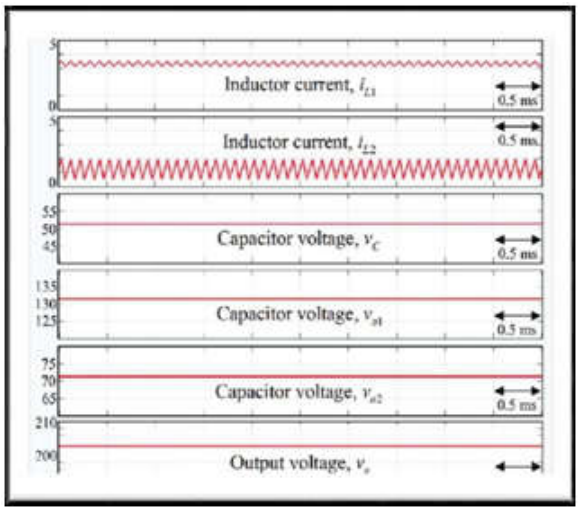
The switches S1 and S2 are turned OFF. Diodes D1 & D2 are in forward biased condition and the diode D3 is reverse biased. L1 provides a closed circuit path and directly connects the load and the supply through the capacitorCO2.Current fw: (i) +Vdc -> L1 -> C -> D1 -> -Vdc

(ii) +Vdc -> D2 -> Load (R0) -> CO2 -> L2 -> D1 -> -Vdc

At the output, the voltage is contributed by both the supply (Vdc) and the capacitor voltage (VCO2). Therefore when the two switches are in the OFF condition voltage boosting takes place. The operating switching frequency is 32 kHz (where the typical switching frequency of MOSFETS is around 25 to 500 kHz.).

A function generator was used to generate a PWM signal for open-loop control. To obtain an output voltage, the duty cycle was manually changed to 70%.

The capacitor values selected for CO1, CO2, C is 2700uF, and the inductor values are chosen to be3mH.



II. Multi-Inverter Inverter

The general structure of the multilevel inverter is to provide desired alternating voltage level at the output using several levels of voltages which are usually obtained from capacitor voltage switches in [12-14].

Diode-clamped multilevel inverter (neutral point inverters):

The diode-clamped multilevel inverter employs clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels. This paper is done for 3,5,7 & 9 levels.

Converter type	Diode clamp
Main switching devices	(m-1)x2
Main diodes	(m-1)x2
Clamping diodes	(m-1)x(m-2)
Balancing capacitors	0

5-Level Diode-Clamped Multilevel Inverter

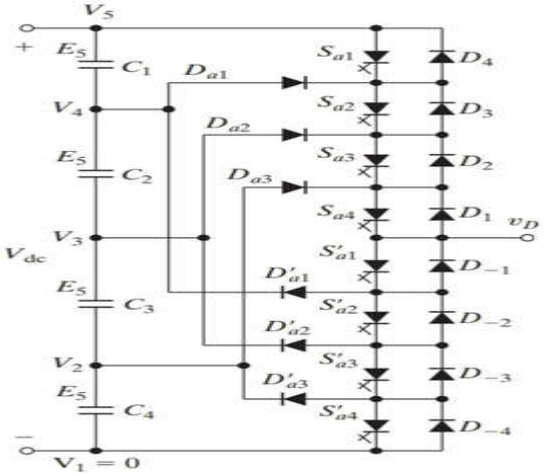


Fig. 5. Circuit of 5 levels DCMLI [15]

Five different levels of output will be obtained by 5 levels diode-clamped multilevel inverter in [7-9].In Five-level DCMLI, the DC bus consists of this capacitors C1, C2, C3, C4. For DC bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clampingdiodesD1, D2, D3, D4, D1', D2', D3'and D4'. Where thrice of D1'equivalent.By suitable switching operations, five different levels of the output voltage are obtained at terminals A and B.Upper switches S1, S2, S3, and S4 are closed and the remaining switches are opened to obtain a voltage of 'Vdc/2' between And B terminals. (VAB =Vdc/2).Upper switches S2, S3, S4 and lower switch S5 are closed and the remaining switches are opened to obtain a voltage of 'Vdc/4' between A and B terminals. (VAB =Vdc/4).To obtain a voltage level VAB=0, close two upper switchesS3 and S4 and two lower switches S5 and S6. (VAB =0).To obtain a voltage level VAB= -Vdc/4, close one upper switch S4 and three lower switches S5, S6, S7. (VAB =-Vdc/4).To obtain a voltage level VAB= -Vdc/2, close all lower switches S5, S6, S7 and S8. (VAB =-Vdc/2)

III. Simulink and Results

The non-isolated chopper is operated with a voltage of 100V dc and 32khz frequency and capacitors 2700micro farad and inductors of 3Mh.

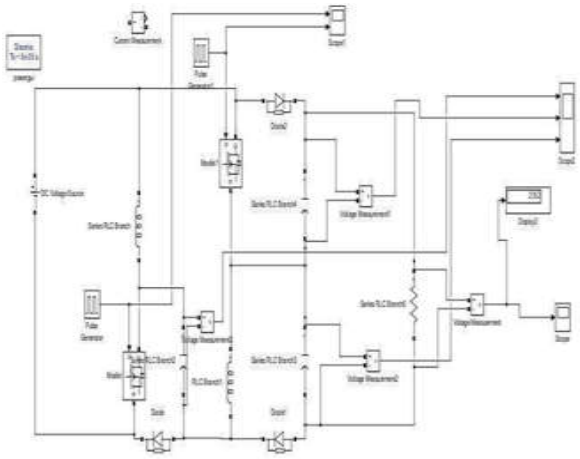


Fig. 6. Simulink model for non-isolated chopper

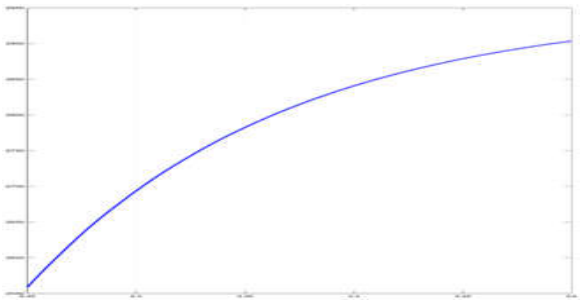


Fig. 7. Output voltage waveform for non-isolated chopper

Fig.6 shows a simulation diagram of a non-isolated chopper diagram. Fig.7 non-isolated converter output voltage. the simulation results were verified in Matlab software.

A. Different Levels Of Diode Clamped Multi-Level Inverter Fed By Non-Isolated Chopper:

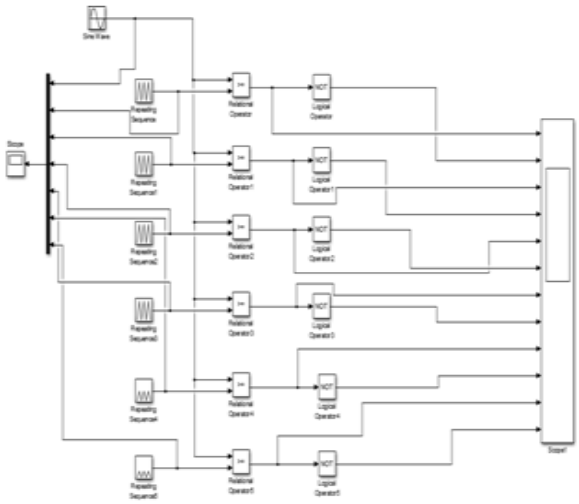
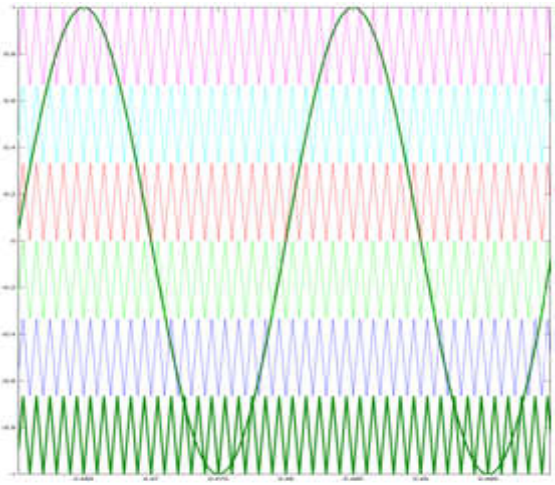


Fig8. Circuit for SPWM Technique (7TH LEVEL)

Fig 9. Waveform for SPWM Technique (7th level)



Similar waveforms are obtained for the 3rd, 5th, and 9th levels

Fig. 8 shows the gate signal generating logic circuit. The presented logic generated pulses for different levels of inverters. When will increase the level of inverter carrier waves also increase and single sinusoidal waveform.

B.5level DCMLI Fed By Non-Isolated Chopper

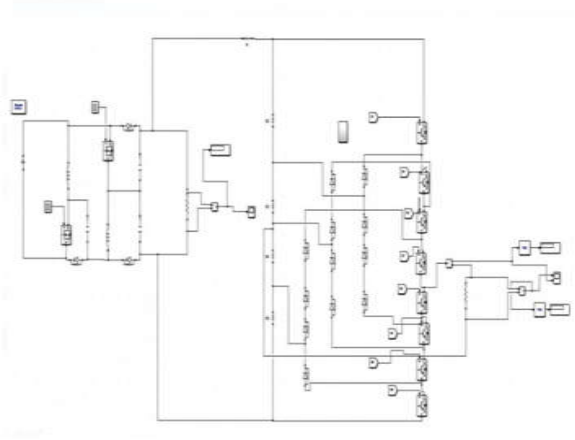


Fig. 10. Simulink diagram for 5 level DCMLI fed by non-isolated chopper

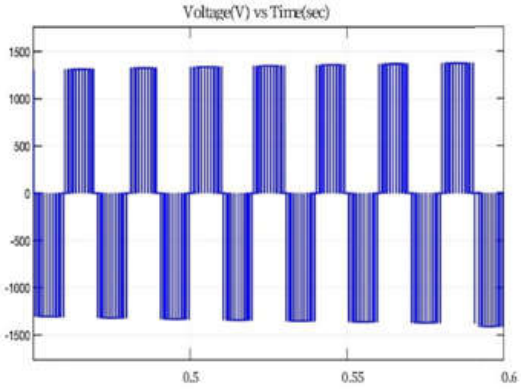


Fig 11. Output voltage waveform for 3 levels DCMLI

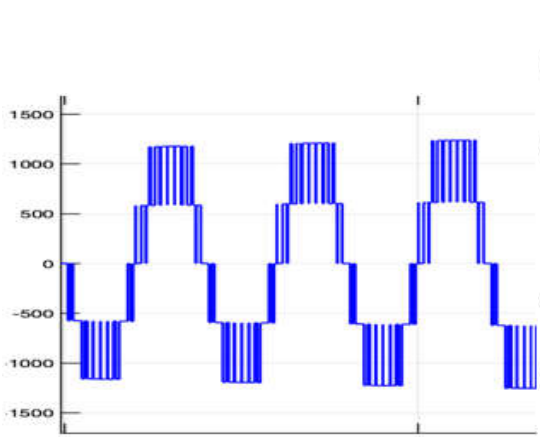


Fig. 12. Waveform for 5 levels DCMLI

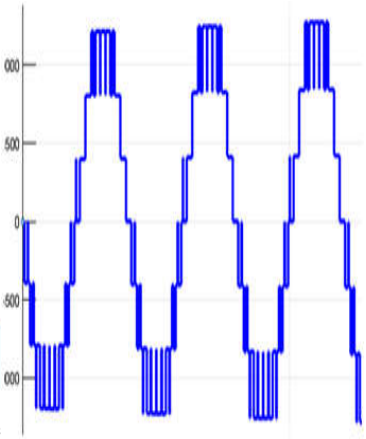


Fig. 13. Output voltage waveform for 7th level

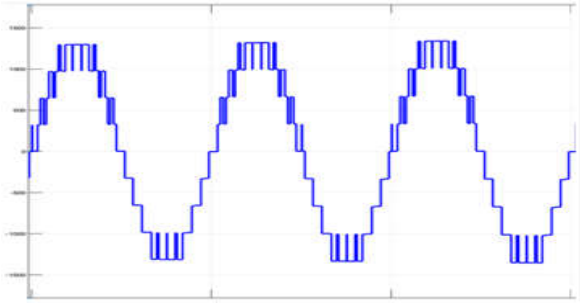


Fig. 14. FFT analysis of THD for 9 level DCMLI

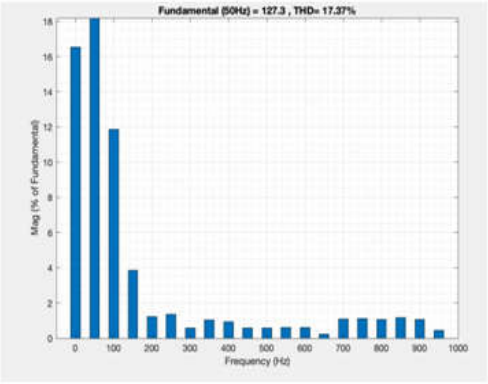


Fig.15 Nine-Level Inverter Output Voltage THD Value

Table.2 Comparison of THD's For Different Levels of Diode Clamped Multi-Level Inverters

Levels of inverter	Percentage of harmonic distortion
3rd level	59.46
5th level	30.94
7th level	21.89
9th level	17.37

Total Harmonic distortion reduced with an increase in the number of levels.

V. Conclusions

The Two-Inductor Non-Isolated Converter fed with different levels of Diode Clamped Multi-level inverters can meet the requirements of high-power quality in industrial applications. The presented topologies simulated in different levels of output voltage. When will increasing levels of output voltage, the system device count also increasing like diodes, power switches and capacitors, as well as reduce THD values in output voltage. Solar PV systems and Electric Vehicles (EV) with lesser harmonic distortions and resolves the increasing world energy crisis for a sustainable future

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