DESIGN AND IMPLEMENTATION OF SEVEN LEVEL MULTILEVEL INVERTER USING RV CONTROL TOPOLOGY WITH HIGH FREQUENCY OF AC POWER DISTRIBUTION

RAJESWARI. R*,V. MOHAN and T. SURESH PADMANABHAN*****

*P.G. Scholar, Dept. of EEE, E.G.S. Pillay Engineering College(Autonomous), Nagapattinam
**Professor and Head, Dept. of EEE, E.G.S. Pillay Engineering College(Autonomous), Nagapattinam
***Professor,Dept. of EEE, E.G.S. Pillay Engineering College(Autonomous), Nagapattinam

Abstract—Multilevel inverters for high-power , high-voltage applications were commonly accepted. Due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages their output is highly superior to that of traditional two-level inverters.However, it also has some drawbacks such as increased number of components, complex method for controlling pulse width modulation, and voltage-balancing issue. A new topology with a reversing-voltage component is proposed in this paper to improve performance at multilevel by compensating for the stated disadvantages.This leads in terms less components than existing inverters (especially in higher levels) and requires fewer carrier signals and gate drives. The overall cost and complexity are therefore greatly reduced particularly for higher output voltage levels. Finally, a prototype of the proposed topology on seven levels is constructed and tested to demonstrate the inverter 's efficiency by experimental results.

***Index Terms*—Multilevel inverter, power electronics, SPWM,topology.**

I. INTRODUCTION

The conversion of multilevel power was initially implemented more than two decades ago. The general principle includes the use of a greater number of active semiconductor switches in small voltage steps to perform the power conversion. This method has some advantages as compared to the traditional power conversion method. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (*dv/dt*) stress on the load and the electromagnetic compatibility concerns [1]. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. Usually, however, the series connation is made with clamping diodes which eliminates

concerns about overvoltage. Moreover, because the switches are not completely connected in sequence, their switching may be staggered, which decreases the switching frequency and hence the losses of switching. A clear downside of multilevel power conversion is the increased number of semiconductor switches needed. It should be noted that lower voltage rating switches can be used in the multilevel converter and therefore the active half-conductor cost is not significantly increased compared to the two level cases. However, each addition of active semiconductors involves related gate drive circuits and adds more complexity to the mechanical layout of the converter. Another drawback of multilevel power converters is that isolated voltage sources or a bank of series capacitors usually produce the small voltage steps.Confined voltage sources can not always be readily available, and voltage balance [2] is required for series condensers. The voltage balance can be solved to some degree by the use of redundant switching states, which occur due to the large number of semiconductor devices. However, another multilevel converter may be needed for a complete solution to the voltage-balancing problem [3]. There has been a major rise in interest in multilevel power conversion in recent years. Recent research has included the development of new topologies for converters, and special modulation strategies. However, the most recent inverter topologies used, which are specifically discussed as valid multilevel inverters, are cascade converters, NPC inverters and flying capacitor inverter. There are also some combinations of the above listed topologies as a two-level converter sequence with a three-level NPC converter called a 3/2 multilevel inverter cascade[4]. There is also a series of a three-level cascade converter with a five-level NPC converter called a multilevel cascade 5/3 inverter. [5]. Some of the requirements for these new converters include industrial drives[6], versatile AC transmission systems (FACTS)[7]–[9], and vehicle propulsion[10],[11]. One field where multi-level converters are especially suitable for renewable photovoltaic energy is that performance and quality of energy are of great concern to researchers[12].Some new methods have recently been proposed, such as the topology of low-frequency high-power switching devices [13]. While the topology has some adjustment to minimize the distortion of the output voltage, the general drawback of this approach is that it has large low-order current harmonics.It is also unable to precisely control the magnitude of the output voltage due to the adopted pulse width modulation (PWM) method[14]. In [15] and [16], a multi-level output is created by a multi-winding transformer. However, the design and manufacture of a multi-winding transformer is complicated and expensive for high-power

applications.A novel four-level inverter topology is also suggested and is appropriate for inverters with an even number of voltage levels and not capable of producing a zero voltage state. As a consequence, the inverter output phase voltage for zero modulation indexes is a bipolar waveform with two distinct values and a high rms value and large harmonic energy concentrated at the switching frequency. This is a disadvantage of the proposed inverter, particularly when it should output low or zero voltage to a load [17]. Another approach is selection based on a set target which can be either the minimum switches used or the minimum used dc voltage. It also requires different voltage source values which are defined according to the target selection [18]. However, this approach also needs basic units which are connected in series, and the basic units still require more switches than the proposed topology. Another disadvantage of the topology is that the power switches and diodes also need to have a different rating which is a major drawback of the topology. In [19], the voltage sources are not used efficiently in generating output voltage levels. For example, the topology in [19] can generate only five output levels with four dc sources, while conventional multilevel inverters can generate up to nine levels with the same number of power supplies.

The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. However, there are asymmetrical topologies [20] which require different voltage sources. This criterion needs to arrange dc power supplies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies [21]–[23], while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage products. In [24], a new approach has been proposed that decreases the number of required dc supplies and inserting transformer instead. The main disadvantage of the approach is adding so many transformer windings which will add up to the overall volume and cost of the inverter.

There is also another topology which requires more switches than the proposed topology for the same number of levels [25]. Some of the proposed topologies suffer from complexities of capacitor balancing [26]–[28]. In [26], the capacitor values used in the topology are proportional to the load current, and as the load current increases, a larger capacitor should be selected. In [27], the capacitor voltage will affect the output voltage when modulation index reaches near its extreme values, i.e., zero or one.

This paper This paper describes the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation and experimental results of the proposed topology are also presented.

2.SEVEN LEVEL MULTILEVEL INVERTER TOPOLOGY (RV)

A new MLI topology named reversing voltage (RV) which requires a smaller number of components when compared to conventional topologies is presented in this project. In this topology, the power conversion is divided into two parts of which one operates at line frequency thereby leading to reduced number of high frequency switches. Hence it has simpler and more reliable control. Switching sequences in this converter are easier than its counter parts. This project describes a seven-level inverter based on reversing voltage topology. The inverter is driven by the general method of multilevel modulation phase disposition SPWM.

In conventional multilevel converters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high frequency switches to generate the required levels. The switches in this part should have high-switching frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output.

3.1.BLOCK DIAGRAM OF PROPOSED SYSTEM

The block diagram of functional MLI using RV topology shown in fig 1. In order to generate a complete multilevel output, the positive Levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the

semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

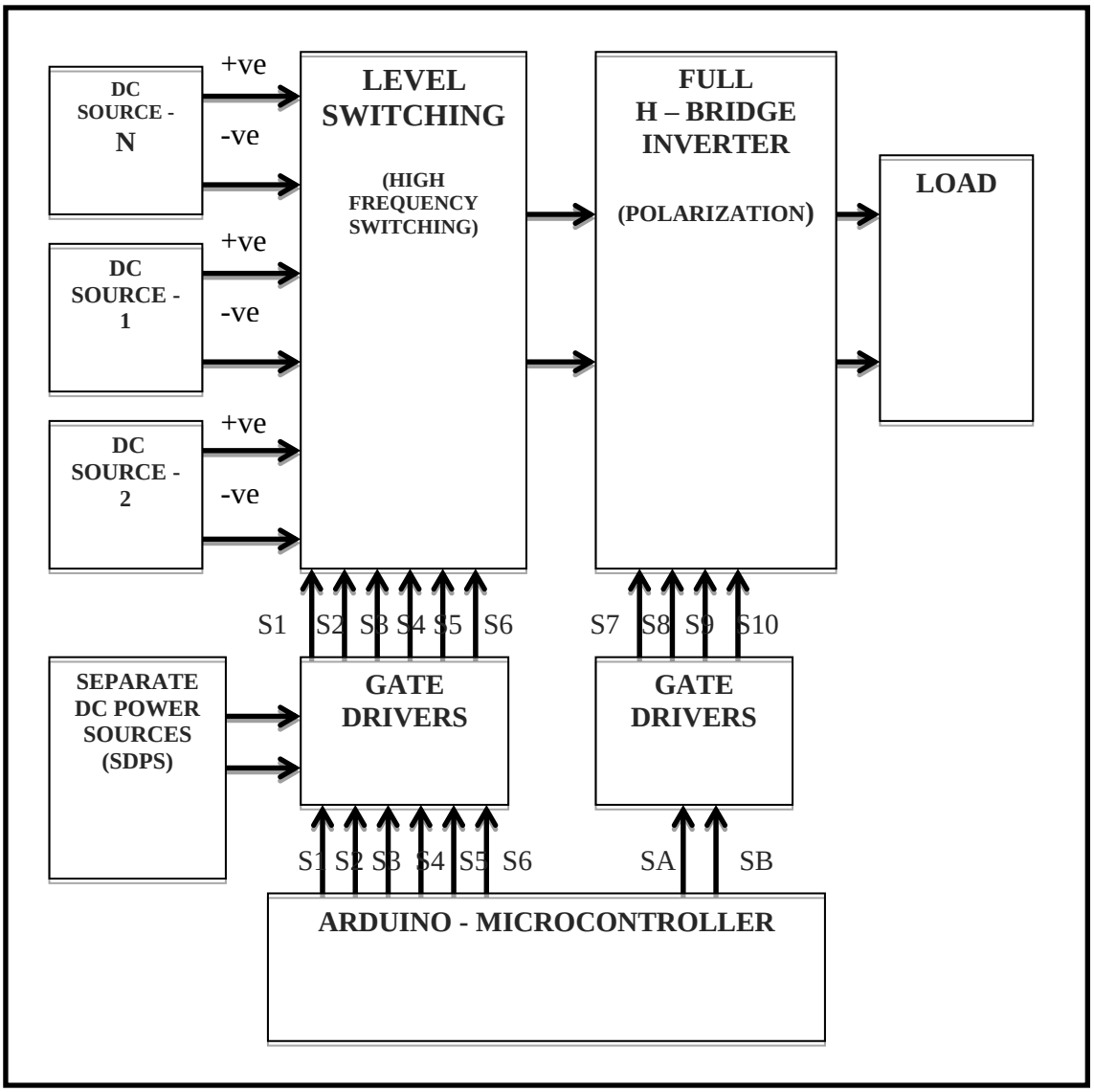


Fig. 1: Block diagram of MLI using RV topology

4. PROPOSED MLI DESING FOR SINGLE PHASE INVERTER

This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. The complete single-phase inverter for seven levels inverter shown in fig.2.

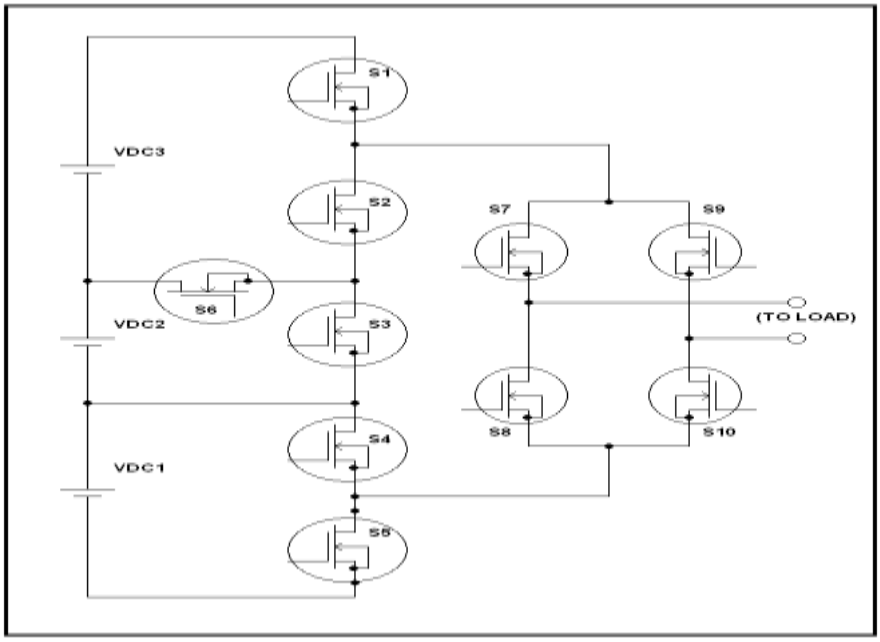


Fig.2: Seven level single phase CHBMLI inverter

The RV topology in seven levels is can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage. This part, which is named polarity generation, transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.

CHBMLI is suitable for high voltage applications because, each H bridge consists of 4 switch and one DC source. Clamping capacitors and diodes are not used here. In CHBMLI Topology, depending upon DC source it consists of two types, 1.Single DC source and 2.Multiple DC source. In Single DC source the CHBMLI are connected in parallel and to the output of each H Bridge the low frequency transformer is connected .To increases the “n” number of levels the Transformer is increased for each H Bridge inverter, so that the efficiency

of system will become less. In multiple DC Source the CHBMLI are connected in series. To increase the “n” number of output voltage levels the several H-Bridge and DC source are used. To reduce the switches in this topology the Symmetrical and Asymmetrical CHBMLI are utilized the number of MOSFET in Symmetrical unit Circuit.

4.1 SWITCHING MODE OPERATION

This topology has easier switching sequences compares to other converter topologies. Generation of negative pulses for negative cycle control is eliminated. Instead, the required level is produced by the level generating part which is the translated to the required polarity according to output voltage requirements. The switching sequence in this topology is redundant and flexible.

4.2 CURRENT FLOW SWITCHING SEQUENCE

The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. For example, a seven-level cascade topology has 12 switches, and half of them, six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.

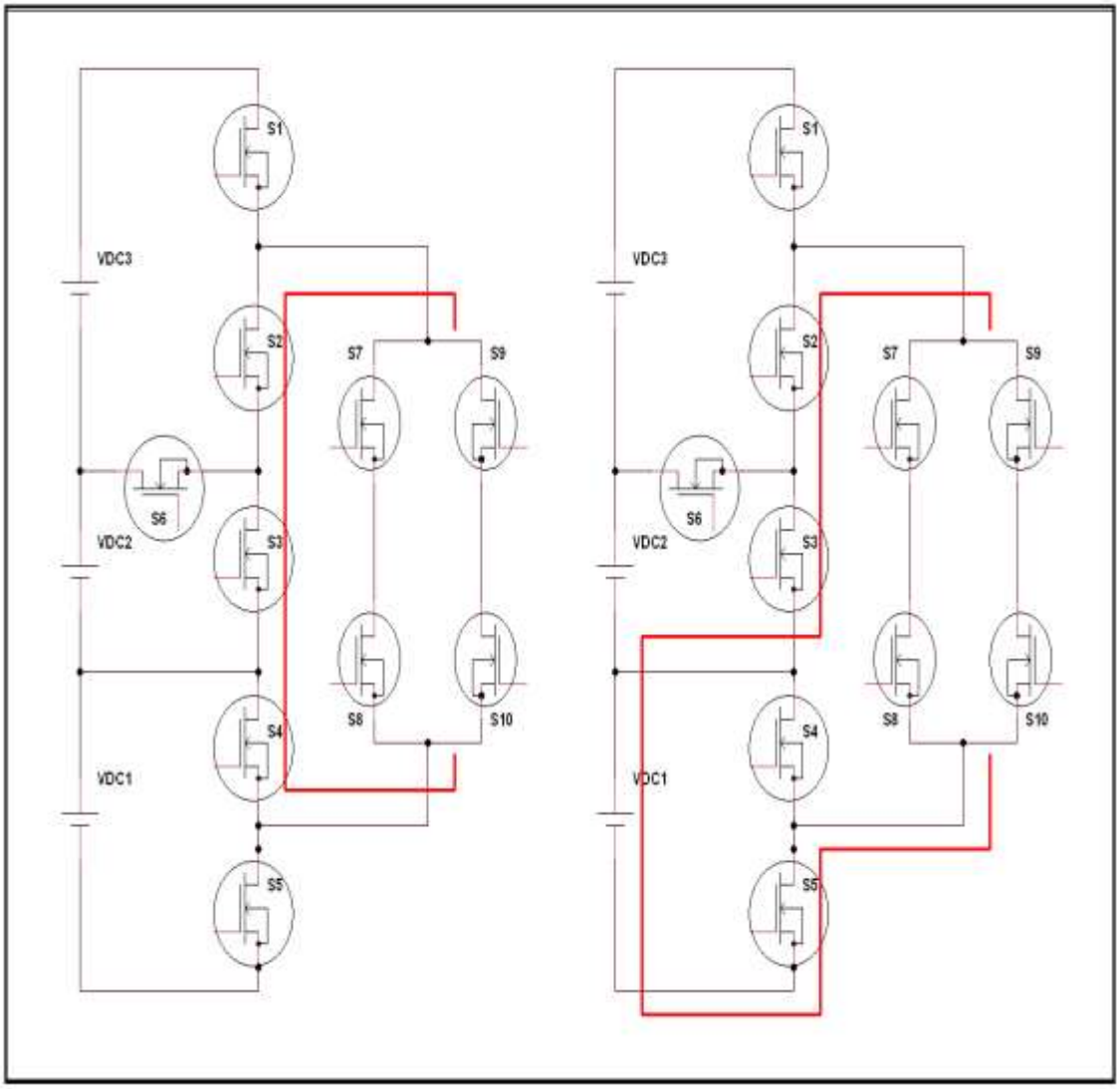


Fig.3: Switching sequence levels 0 & level 1

The sequence of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. As can be observed, this part generates the output voltage levels by appropriate switching sequences. The output voltage is the sum of the voltage sources which are includes in the current path.

The various switching modes in generating the required levels is shown Table 1 below.

Table 1 Switching states in different levels

Levels	Switching Sequence
Level 0	2-3-4
Level 1	2-3-5
Level 2	2-3-6
Level 3	1-5

5. Results and Discussion

5.1 Matlab Analysis

MATLAB (Matrix Laboratory) is a special-purpose computer program optimized to perform engineering and scientific calculations. It is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation

5.2 Simulation Results

Some simulation tests have been carried out using MATLAB/Simulink for single phase seven-level CHB inverter to evaluate the feasibility of the SHM-PAM technique and the obtained results. The parameters used in the simulation are: the nominal voltage for each separated DC sources, Vdc=100 V,. The voltage across the capacitor C1, would always be constant at 24 V. As well, the frequency of output voltage is 50 Hz. The simulation results have been presented for to prove that the pulses width are constants while the value of m_a changes. Simulation circuit for seven level CHB and corresponding output shown in fig 4 and 5

5.3 Harmonic Analysis

This paper has presented Total Harmonic Distortion (THD) analysis for Symmetric Cascaded Multilevel Inverter (SCMLI). Here comparative study is done from 5th level to

25th level for output voltage and load current. The harmonic contents are analyzed up to 7th harmonics in various levels of outputs shown in figure 6.

5.4 SIMULINK MODEL OF SEVEN LEVEL CASCADED H- BRIDGE INVERTER

SPWM is adopted for switching due to its simplicity. An ATmega 16 is programmed to generate the necessary gate pulses for the switches. The Arduino provides an output signal that typically is limited to a few milliamperes of current. Hence, the transistor will take quite some time to switch leading to power loss. Also, the gate capacitor of transistor causes a current overdraw during switching as it draws current quickly. This causes overheating which leads to permanent damage or even complete destruction of the chip. A gate driver is used to prevent this problem.

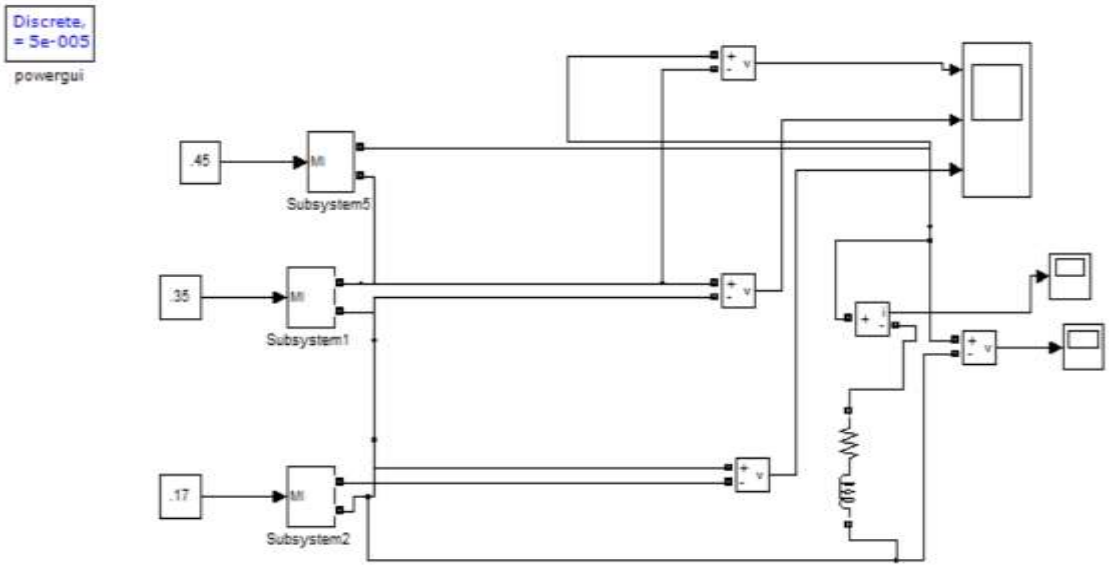


Fig.4: Simulink model of seven level CHBMLI

SIMILATION DIAGRAM

Simulation diagram of the proposed system is show in fig. . The THD anysis of output voltage for 21- level SCMLI also shown in fig 6.

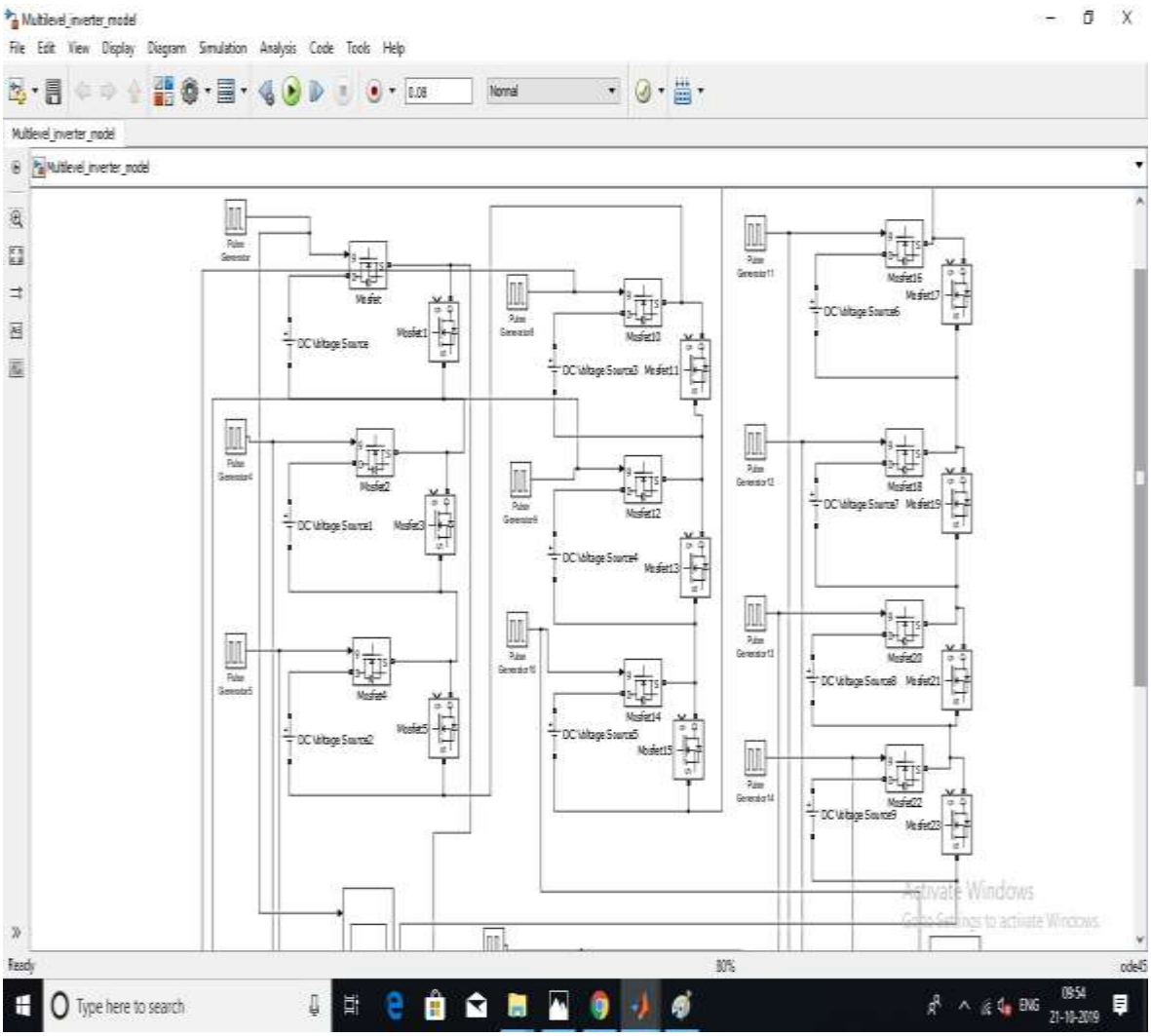


Figure 5 Simulink model

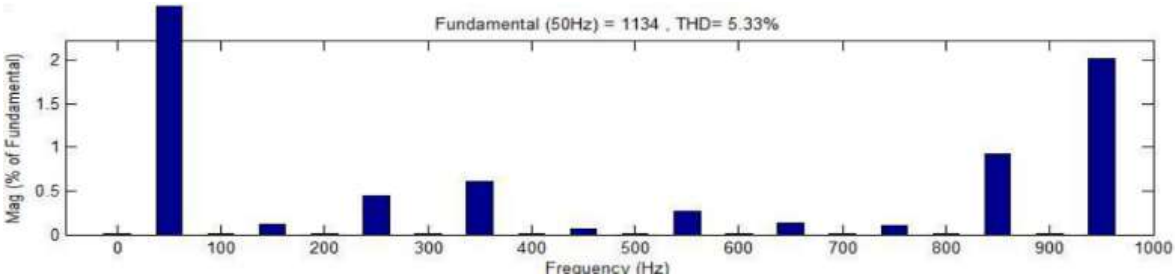


Fig.6: THD anysis of output voltage for 21- level SCMLI

Seven level multilevel inverter scope 1 output

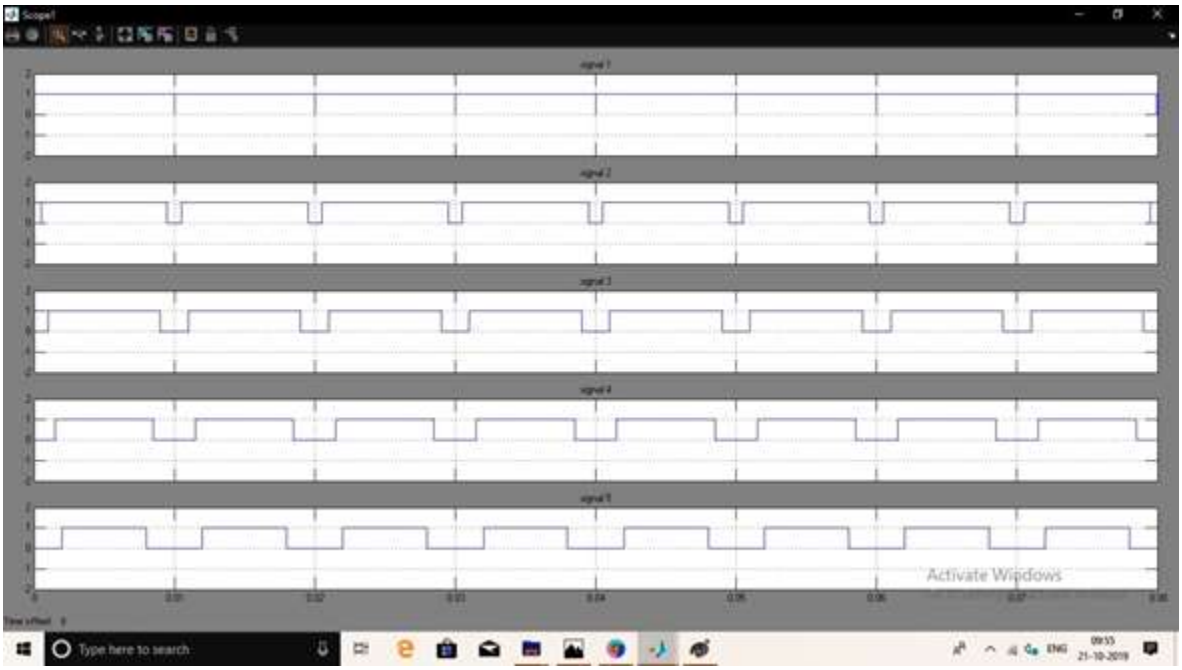


Fig.7: Seven level Multilevel inverter Pulse generated Wave form

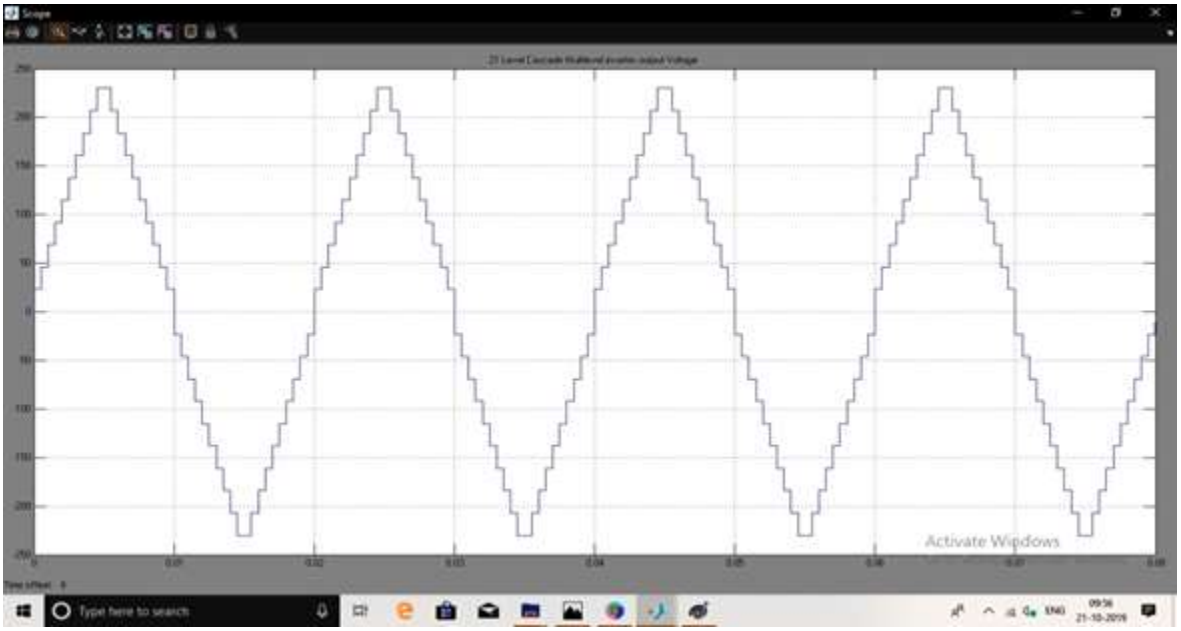
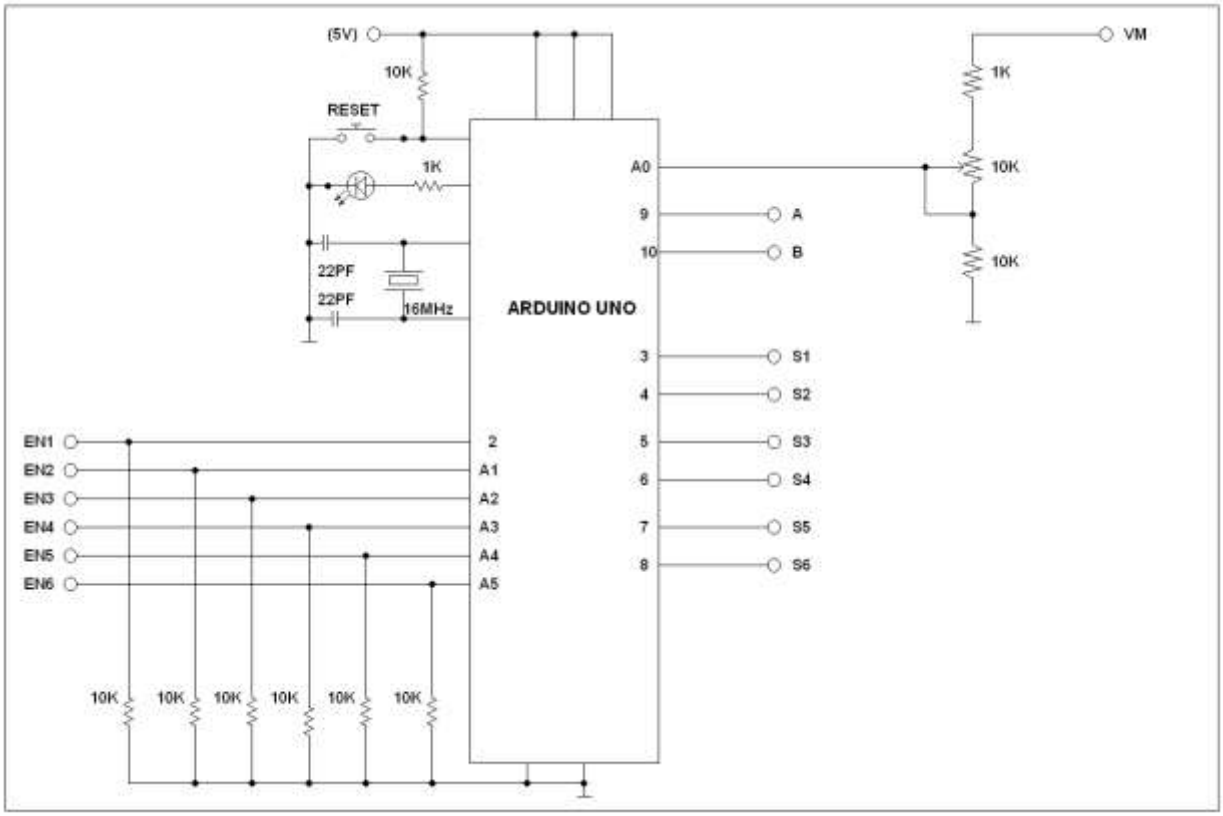
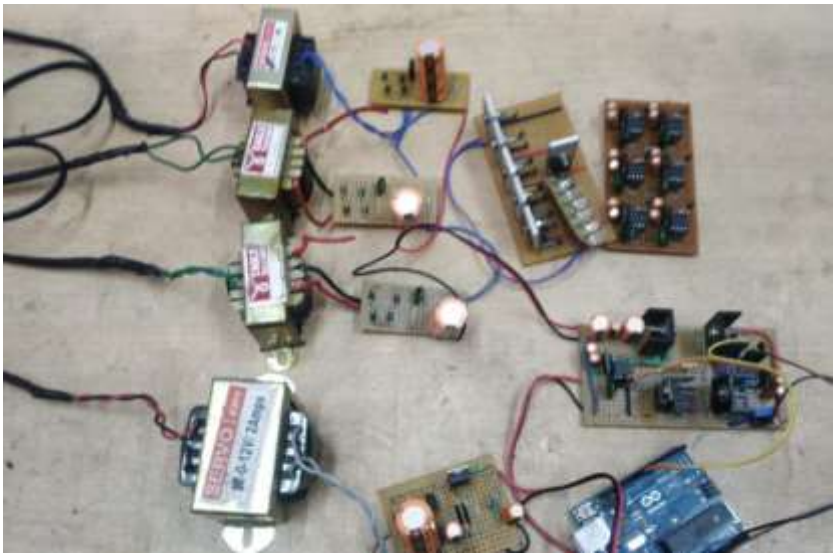


Fig.8: load output voltage wave form



(a)



(b)

Fig. 9: Experimental setup (a)Circuit connection (b) Hardware module

CONCLUSION

It has been observed from the simulation results that the overall efficiency of the developed seven level inverter is 95% which is more than the conventional DC to AC inverter. The design of the 7-level multilevel inverters seems to be better than the 9-level multilevel inverters. The concept of multilevel inverter by increasing the number of levels reduces the total harmonic distortion of the system and improving the power quality. The reversing voltage topology is based on the principle idea of generating the output waveform in the positive polarity and then feeding it to a full bridge inverter to produce the output waveform in both positive and negative polarity. By doing so, the required number power switches are reduced. Also, this topology has superior features in terms of isolated supply, control requirements, cost, and reliability. Since the switching is divided into high frequency and low frequency, the efficiency is improved, and its cost is reduced by increasing the number of levels, the cost and weight of the multilevel inverter will be increased. So this topology is well suited for industrial drives

REFERENCES

[1] K. Jang-Hwan, S.-K.Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltagesource inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.

[2] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[3] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[4] T. L. Skvarenina, *The Power Electronics Handbook*. Boca Raton, FL: CRC Press, 2002.

[5] X. Yun, Y. Zou, X. Liu, and Y.He, "A novel composite cascade multilevel converter," in *Proc. 33rd IEEE IECON*, 2007, pp. 1799–1804.

[6] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. 34th IEEE IAS Annu. Meeting*, 1999, vol. 4, pp. 2662–2669.

[7] E. Najafi and A. H. M. Yatim, “A novel current mode controller for a static compensator utilizing Goertzel algorithm to mitigate voltage sags,” *Energy Convers.Manage.*, vol. 52, no. 4, pp. 1999–2008, Apr. 2011.

[8] N. Seki and H. Uchino, “Converter configurations and switching frequency for a GTO reactive power compensator,” *IEEE Trans. Ind. Appl.*, vol. 33, no. 4, pp. 1011–1018, Jul./Aug. 1997.

[9] G. Shahgholiyan, E. Haghjou, and S. Abazari, “Improving the mitigation of voltage flicker by usage of fuzzy control in a distribution static synchronous compensator (DSTATCOM),” *Majlesi J. Elect. Eng.*, vol. 3, no. 2, pp. 25–35, Jun. 2009.

[10] K. Nakata, K. Nakamura, S. Ito, and K. Jinbo, “A three-level traction inverter with IGBTs for EMU,” in *Conf. Rec. IEEE IAS Annu. Meeting*, 1994, vol. 1, pp. 667–672.

[11] A. Jidin, N. R. N. Idris, A. H. M. Yatim, T. Sutikno, and M. E. Elbuluk,“An optimized switching strategy for quick dynamic torque control in DTC-hysteresis-based induction machines,” *IEEE Trans. Ind. Electron.*,vol. 58, no. 8, pp. 3391–3400, Aug. 2011.

[12] K. Y. Lau, M. F. M. Yousof, S. N. M. Arshad, M. Anwari, and A. H. M. Yatim, “Performance analysis of hybrid photovoltaic/diesel energy system under Malaysian conditions,” *J. Energy*, vol. 35, no. 8, pp. 3245–3255, Aug. 2010.

[13] G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi, “Three-phase lowfrequency commutation inverter for renewable energy systems,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1522–1528, Oct. 2006.

[14] S. Daher, J. Schmid, and F. L. M. Antunes, “Multilevel inverter topologies for stand-alone PV systems,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.

[15] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, “Multilevel inverter by cascading industrial VSI,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832–838, Aug. 2002.

[16] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, “A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter,” in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[17] G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, “A novel four-level voltage source inverter-influence of switching strategies on the distribution of power losses,” *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 149–159, Jan. 2007.

[18] E. Babaei, “Optimal topologies for cascaded sub-multilevel converters,” *J. Power Electron.*, vol. 10, no. 3, pp. 251–261, May 2010. [19] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, “A reducedswitch- count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2344–2351, Aug. 2007.

[20] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, “Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source,” *J. Power Electron.*, vol. 10, no. 2, pp. 138–145, Mar. 2010.

[21] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, “A new simplified multilevel inverter topology for dc-ac conversion,” *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[22] N. A. Rahim, K. Chaniago, and J. Selvaraj, “Single-phase seven-level grid-connected inverter for photovoltaic system,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[23] J. Selvaraj and N. A. Rahim, “Multilevel inverter for grid-connected PV system employing digital PI controller,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[24] S. G. Song, F. S. Kang, and S.-J. Park, “Cascaded multilevel inverter employing three-phase transformers and single dc input,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[25] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, “Active neutral-point-clamped multilevel converters,” in *Proc. IEEE 36th Power Electron Spec. Conf.*, 2005, pp. 2296–2301.

[26] S. A. Gonzalez, M. I. Valla, and C. F. Christiansen, “Analysis of a cascade asymmetric topology formultilevel converters,” in *Proc. IEEE ISIE*, 2007, pp. 1027–1032.

[27] P. Lezana and J. Rodriguez, “Mixed multicell cascaded multilevel inverter,” in *Proc. IEEE ISIE*, 2007, pp. 509–514. [28] R. Stala, “Application of balancing circuit for dc-link voltages balance in a single-phase diode-clamped inverter with two three-level legs,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4185–4195, Sep. 2011.

[29] C. Govindaraju and K. Baskaran, “Analysis and implementation of multiphase multilevel hybrid single carrier sinusoidal modulation,” *J. Power Electron.*, vol. 10, no. 4, pp. 365–373, Jul. 2010.

[30] A. Radan, A. H. Shahirinia, and M. Falahi, “Evaluation of carrier-based PWM methods for multi-level inverters,” in *Proc. IEEE ISIE*, 2007, pp. 389–394.

[31] Y.-M. Park, H.-S.Ryu, H.-W.Lee, M.-G.Jung, and S.-H. Lee, “Design of a cascaded H-bridge multilevel inverter based on power electronics building blocks and control for high performance,” *J. Power Electron.*, vol. 10, no. 3, pp. 262–269, May 2010.

[32] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pe´rez, “A survey on cascaded multilevel inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[33] C. Cecati, F. Ciancetta, and P. Siano, “A multilevel inverter for photovoltaic systems with fuzzy logic control,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, Dec. 2010.

[34] G.-J. Su, “Multilevel dc-link inverter,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May/Jun. 2005.

[35] J.-S. Lai and F. Z. Peng, “Multilevel converters-a new breed of power converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[36] C. A. C. Cavaliere, E. H. Watanabe, and M. Aredes, “Multi-pulse STATCOM operation under unbalanced voltages,” in *Proc. IEEE Power Eng. Soc. Winter Meeting*, 2002, vol. 1, pp. 567–572.

[37] S. Halasz, G. Csonka, A. A. M. Hassan, and B. T. Huu, “Analysis of the unipolar PWM techniques,” in *Proc. 8th MELECON*, 1996, vol. 1, pp. 353–356.